Mini PCI Specification

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Chapter 1
Introduction

1.1 Overview

The Mini PCI Specification defines an alternate implementation for small form factor PCI cards referred to in this specification as a Mini PCI Card. This specification uses a qualified sub-set of the same signal protocol, electrical definitions, and configuration definitions as the *PCI Local Bus Specification*.

Where this specification does not explicitly define PCI characteristics, the *PCI Local Bus Specification* governs.

The primary differences between a standard PCI expansion card and a Mini PCI Card are:

- The form factor of the card and card-system interconnection, that is, the smaller physical size of the Mini PCI Card and the connectors it uses
- The use of standard sideband signals for audio and communications
- Support of the **CLKRUN#** signal defined in the *PCI Mobile Design Guide*
- No support for optional JTAG signals, nor for the 64-bit PCI extension defined in the *PCI Local Bus Specification*

1.2 Motivation

The performance characteristics of the PCI local bus, demonstrated in desktop and server systems, make PCI cards desirable in a wide range of systems. Proprietary form factor PCI cards are already commonplace, underscoring the need for a standard to simplify designs, reduce costs, and increase the number of implementation options.

This specification defines a standard small-form-factor card (using the 32-bit PCI local bus) that can be used in smaller systems in which standard PCI and Small PCI expansion cards cannot be used due to mechanical system design constraints. Examples of such smaller systems include notebook PCs and docking stations, sealed-case PCs (Net PCs or NCs), and set top boxes integrating communications capabilities. Figure 1-1 is a logical representation of the Mini PCI Specification.

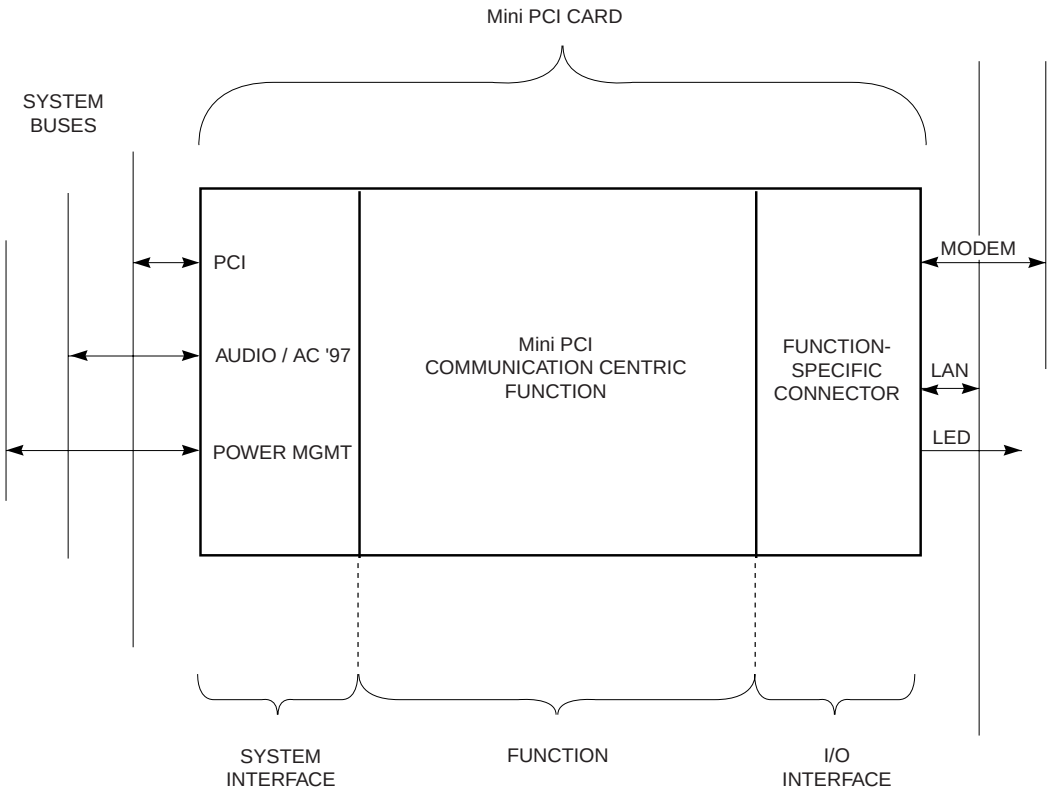

Figure 1-1: Logical Representation of the Mini PCI Specification

Figure 1-2 shows a cutaway view of a notebook computer with a Mini PCI Card installed. The illustration shows a conceptual placement of the card. Actual installation location depends on the manufacturer.

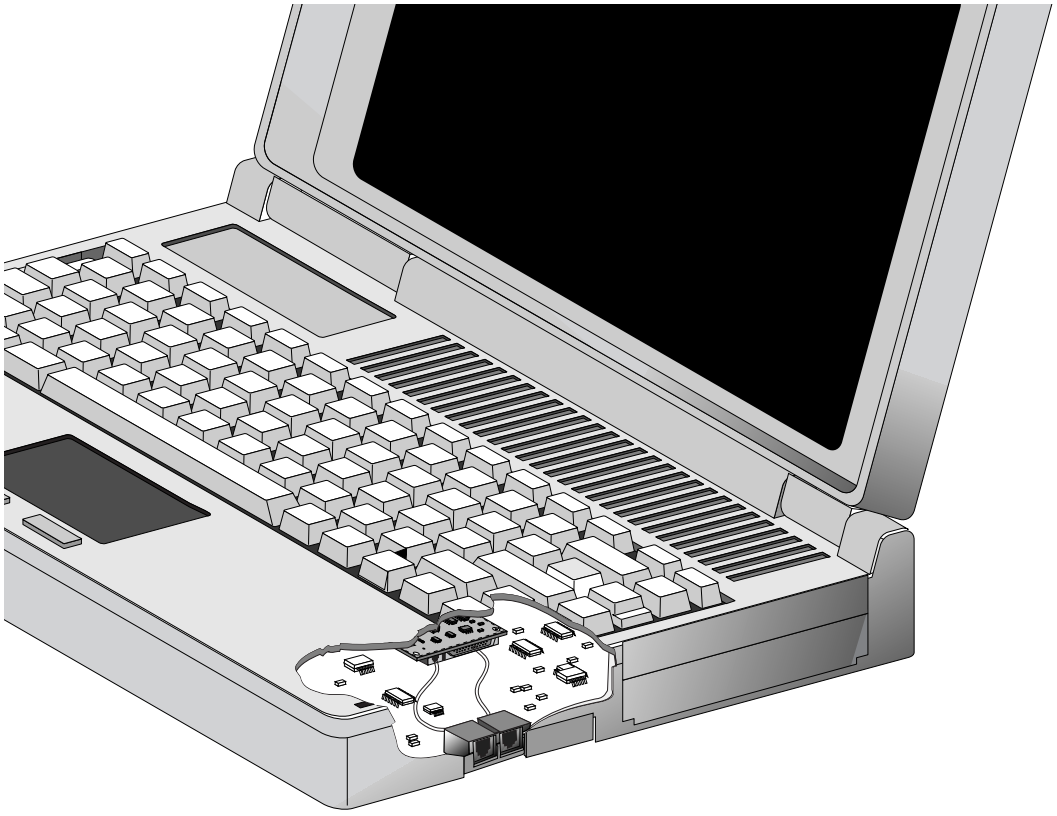

Figure 1-2: Type I/Type III Mini PCI Card in a Notebook Computer

1.3 Features and Benefits

This specification establishes a high-performance local-bus standard for small or restricted mechanical environments. The key features and benefits can be divided into two groups.

The first group of benefits comes from the use of an alternate form factor:

- **Upgradeability.** Mini PCI Cards are removable and upgradeable with available "new technology" cards. This allows upgrades to the newest technologies. Where required, it is the system manufacturer's responsibility to provide sufficient notification in the accompanying manual that service should be performed by a qualified technician.
- **Flexibility.** A single Mini PCI interface can accommodate various types of communications devices. Therefore, the OEM manufacturer can supply "build to order" systems (for example, a network interface card instead of a modem or Token Ring instead of Ethernet).
- **Reduced Cost.** A standard form factor for small form factor cards makes them more manufacturable, which reduces costs and provides economies-of-scale advantage over custom manufactured form factors.

- **Serviceability.** Mini PCI Cards can be removed and easily serviced if they fail.
- **Reliability.** Mini PCI Cards will be mass produced and, consequently, of higher quality than low-volume custom boards.
- **Software Compatibility.** Mini PCI Cards are intended to be fully compatible with existing software drivers and applications developed for standard PCI expansion cards. In addition, it is strongly recommended that all Mini PCI Cards support current industry standards such as the applicable version of the *PC XX System Design Guide* (currently at version PC 99), *Advanced Configuration and Power Interface Specification* (ACPI), and other industry initiatives that may be developed in the future.
- **Reduced Size.** Mini PCI Cards are smaller than PCMCIA cards, Small PCI cards, and typical daughter boards. This reduced size permits a higher level of integration of data communications devices into notebook PCs, docking stations, sealed-case PCs (NetPCs or NCs), and set top boxes. Figure 1-3 shows a size comparison between the Type I Mini PCI Card and a standard PCI expansion card.
- **Regulatory Agency Accepted Form Factor.** Standardization of the Mini PCI Card form factor will permit world wide regulatory agencies to approve Mini PCI communications devices independent of host systems. This significantly reduces cost and risk on the part of systems manufacturers.

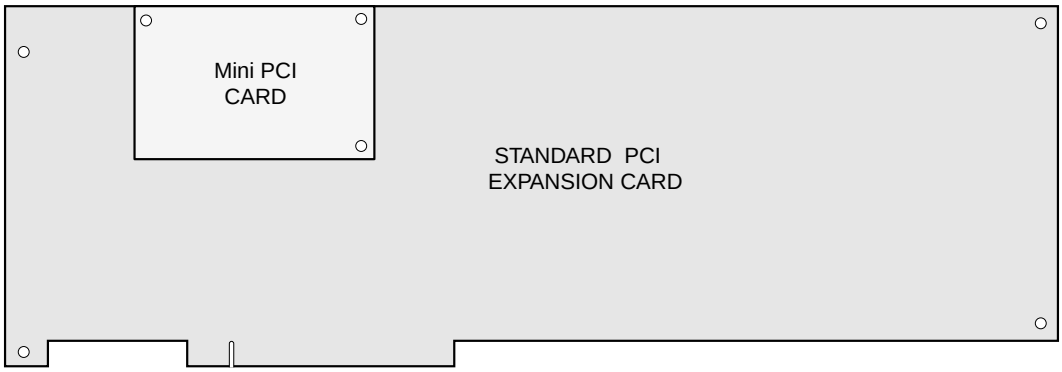

Figure 1-3: Mini PCI and Standard PCI Size Comparison

The second group of benefits derives from the use of the high-performance PCI local bus:

- **High Performance.** The PCI high-performance characteristics include 32-bit data path, full concurrency with the processor and memory subsystem, and hidden (overlapped) central arbitration.
- **Ease of Use.** Mini PCI supports full auto-configuration of PCI local bus add-in boards and components.
- **Longevity.** Implementing subsystems on the Mini PCI Cards increases system board utility. PCI local buses are processor independent and support multiple families of processors and future generations of processors (by bridges or by direct integration).
- **Flexibility.** PCI's full multi-master capability allows any PCI master peer-to-peer access to any PCI master/target.
- **Data Integrity.** PCI provides parity on both data and address and allows implementation of robust client platforms.
- **Power Management.** Consideration for mobile systems power requirements, PCI bus power management, and clock run protocol support.

1.4 Specification References

This specification should be used in conjunction with the following specifications and documents (which were at the corresponding version numbers at the time of writing):

- *PCI Local Bus Specification, Revision 2.2*
- *PCI Bus Power Management Interface Specification, Revision 1.1*
- *PCI Mobile Design Guide, Version 1.1*
- *Audio Codec '97 Component Specification, Revision 2.1*
- *PC Card Standard Electrical Specification, Revision April 1998*
- *ISO/IEC 8802-3 ANSI IEEE Standard 802.3*
- *Supplement to ANSI/IEEE 802.3 Document 802.3u*
- *ISO/IEC 8802-5 ANSI IEEE Standard 802.5*

Design considerations should adhere to the guidelines established in the applicable revision of the *PC XX System Design Guide* (currently at version PC 99).

1.5 Administration

This document is maintained by the PCI SIG. The PCI SIG, an unincorporated association of members of the microcomputer industry, was established to monitor and enhance the development of the PCI local bus.

SIG membership is available to all applicants within the microcomputer industry. Benefits of membership include:

- Ability to submit specification revisions and addendum proposals
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- Automatically receive revisions and addenda
- Voting rights to determine the Steering Committee membership
- Vendor ID number assignment
- PCI technical support
- PCI support documentation and materials
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- Participation in the compliance program including participation at the "PCI Compliance Workshops" and the opportunity to be included in the "PCI Integrator's List"

For information on how to become a SIG member or on obtaining PCI local bus documentation, please contact:

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Chapter 2
Signal Definition

2.1 PCI Local Bus Specification References

The Mini PCI Card system interface implements the following:

- A qualified sub-set of the signals required by a PCI interface. Bridging is supported but must be implemented without the **LOCK#** signal.
- Some optional PCI signals.
- A number of additional sideband signals.

Because the Mini PCI Card system interface is implemented with a supply voltage (Vcc) of 3.3 volts, and the bus interface signals are 3.3 volts, there is no requirement that the Mini PCI Card implement a 5 volt tolerant bus interface architecture. The Mini PCI signal set can be divided into three sub-sets:

- PCI interface
- PCI power management
- Sideband

Sideband signals provide audio and communications support.

2.2 System Connector Interface Signals

The Mini PCI Card PCI interface signal sub-set is defined in Figure 2-1.

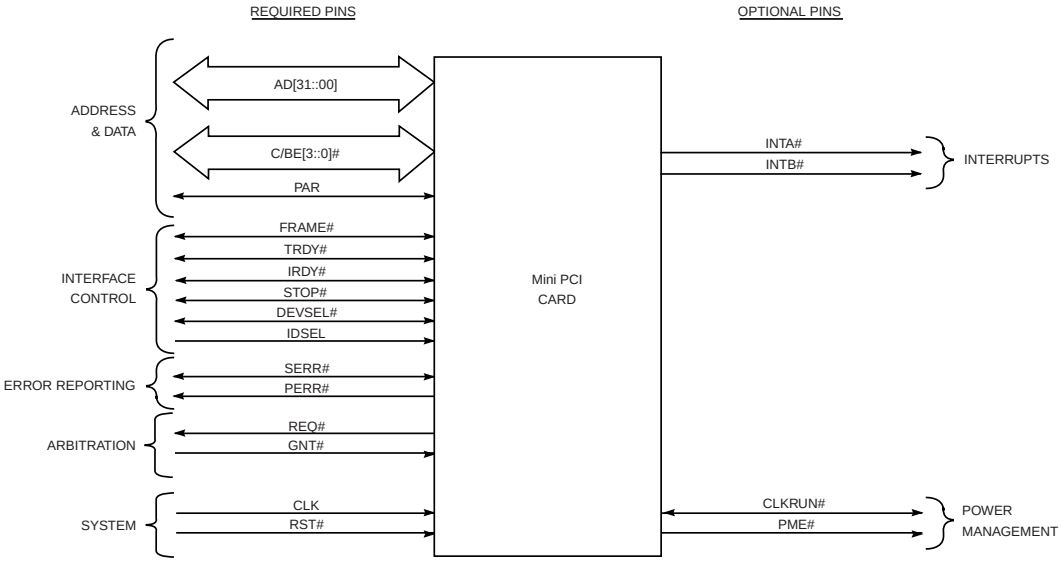


Figure 2-1: Mini PCI Card System PCI Signal Set

The signals follow the specifications as defined in Chapter 2 of the *PCI Local Bus Specification.* All signal directions are specified with respect to the system board.

Mini PCI power management consists of the following:

- PCI power bus management signals **PME#** and **3.3VAUX** as defined in the *PCI Bus Power Management Interface Specification,* with the exceptions noted in Chapter 7 of this document
- **CLKRUN#** as defined in the *PCI Mobile Design Guide*

This specification does not require that the system board implement Mobile PCI's clock run. If clock run is not implemented on the system board, the clock run pin on the system connector must be terminated low on the system board. This specification does require that the Mini PCI Card implement clock run functionality. Functionality does not allow for terminating the **CLKRUN#** pin to ground or through a pull-down resistor to indicate that the Mini PCI Card cannot tolerate a stopped or slowed clock. If the Mini PCI Card cannot tolerate the clock stopping or slowing, the Mini PCI Card must implement the clock run protocol and indicate that the clock cannot be stopped according to the *Mobile PCI Design Guide*. Only if the Mini PCI Card can tolerate the clock being stopped or slowed at any time without notification and the Mini PCI Card will never need to restart the clock, can the Mini PCI Card implement clock run as a no connect.

Clock run cannot be implemented with a static pull-down or repetitive pulse circuit. The protocol must be supported or the implementation must be insensitive to clock stopping or slowing down.

Telephony audio support is provided by the SYS_AUDIO_IN, SYS_AUDIO_OUT, and the MOD_AUDIO_MON pins. Future modem support is available using the *Audio Codec '97 Component Specification* interface.

These signals are shown in Table 2-1. All signal directions are specified with respect to the system board.

Table 2-1: Mini PCI Sideband Signals

Signal Group	Signal	Direction	Description
Power Management Support	**3.3VAUX**	Output	Auxiliary 3.3Vcc support for **PME#**
	CLKRUN#	Input/Output	Control signal for PCI **CLK**. Used to stop or start the PCI clock for power management purposes. Also used to indicate the requirement for re-starting the clock or indicating that the PCI function cannot tolerate stopping the PCI clock.
	PME#	Input	Control signal indicating a power management event has occurred.
	MPCIACT#	Input	Mini PCI function active. Intended to indicate, when low, that the Mini PCI Card is in a communicating state requiring full system performance; for example, a software modem in the off hook state.
AC-link Support	AC_SYNC	Output	Audio Codec '97
	AC_SDATA_IN	Input	Audio Codec '97 This corresponds to the SDATA_INx pin of the AC-link specification where "x" is 0, 1, 2, or 3. It is the responsibility of the system designer to properly connect the AC_SDATA_IN pin to the correct SDATA_IN pin of the system. If the system requires that the codec on the Mini PCI Card be a primary codec, then the system must hook the AC_SDATA_IN pin to SDATA_IN0 on the system board. If the system requires that the codec on the Mini PCI Card be a secondary codec, the system must hook the AC_SDATA_IN pin to the proper SDATA_INy pin on the system board where "y" is 1, 2, or 3.

Table 2-1. Mini PCI Sideband Signals (continued)

Signal Group	Signal	Direction	Description
AC-link Support	AC_BIT_CLK	Input/Output	Audio Codec '97
	AC_ CODEC_ID0#, AC_CODEC_ID1#	Output	Audio Codec '97 Used to assign the Mini PCI AC, AMC, or MC codec to the correct primary or secondary codec address. The system board manufacturer sets these bits based on the connection of AC_SDATA_IN to its respective SDATA_INx pin. A logic high voltage should be tied to the Wake voltage of the Mini PCI Card (3.3VAUX or 3.3V if 3.3VAUX is not used) Connection ID1 ID0 SDATA_IN0 0 0 SDATA_IN1 0 1 SDATA_IN2 1 0 SDATA_IN3 1 1 Note that the pins are logically TRUE when low.
	AC_SDATA_OUT	Output	Audio Codec '97
	AC_RESET#	Output	Audio Codec '97
Audio Support	AUDIO_GND	Output	Analog ground for line level audio
	MOD_AUDIO_MON	Input	Modem audio monitor
	SYS_AUDIO_IN	Input	Telephony audio support
	SYS_AUDIO_OUT	Output	Telephony audio support
	SYS_AUDIO_IN_GND[1]	Input	Return for SYS_AUDIO_IN
	SYS_AUDIO_OUT_GND[1]	Output	Return for SYS_AUDIO_OUT
Phoneline Interface	TIP[1]	Input/Output	Analog phoneline interface for modems
	RING[1]	Input/Output	Analog phoneline interface for modems
LAN Interface	See Table 2-4 for signal assignments[1]	Input/Output	LAN and LAN LED connections
Analog Power	VCC5VA[1]	Output	5 volt power for analog voice circuits

A number of pins are defined as "RESERVED." These pins are reserved for future expansion and must not be connected on the Mini PCI Card or the host platform.

[1] Available on the system connector in the Type III form factor only.

The signals denoted Audio Codec '97 constitute audio support as defined in the *Audio Codec '97 Component Specification.* The host platform support of AC link signals is optional. If AC link signals are supported, the host platform may need to terminate, with weak pulldowns or pullups as required by the system board chipset, the AC_BIT_CLK and AC_SDATA_IN signals to cover instances where the Mini PCI Card is not present or where it does not support AC link. Host platforms not supporting AC-link shall terminate the following signals to ground with less than or equal to 10 kohm termination: AC_RESET#, AC_BIT_CLK, AC_SYNC, and AC_SDATA_OUT. Host platforms not supporting AC-link shall terminate the following signals to Wake voltage with less than or equal to 100 kohm termination: AC_CODEC_ID0# and AC_CODEC_ID1#.

Interrupt support is indicated by PCI interrupts **INTA#** and **INTB#**. PCI 66 MHz bus clock support is provided by **M66EN**. The PCI interrupts and **M66EN** are defined in Chapter 2 of the *PCI Local Bus Specification*.

As a system board device, Mini PCI interrupt support implements some of the latitude afforded system board devices in interrupt assignments as defined in the *PCI Local Bus Specification,* Section 2.2.6.

2.2.1 Modem and System Audio Support

The MOD_AUDIO_MON signal supports Pulse Width Modulation (PWM) modem call progress monitoring. Implementation of the MOD_AUDIO_MON (Modem Audio Monitor) is defined in the *PCMCIA PC Card Standard–Electrical Specification,* Section 5.2.12. The MOD_AUDIO_MON signal is required for data/fax (non-voice) only modem implementations. However, this signal is optional for the purposes of call progress monitoring in voice/data/fax modem implementations.

The definitions for SYS_AUDIO_IN (system audio input from the Mini PCI Card) and SYS_AUDIO_OUT (system audio output to the Mini PCI Card) are line-level audio signals intended to support modem speakerphone type implementations. These signals are required for voice/data/fax modem implementations. These signals are optional for data/fax only modem implementations. Examples are shown in Figures 4-1 and 4-2. The electrical parameters of SYS_AUDIO_IN and SYS_AUDIO_OUT can be found in Chapter 4 of this document.

The Type III Mini PCI form factor has two additional signals, SYS_AUDIO_IN_GND and SYS_AUDIO_OUT_GND, which may be used to support different audio implementations. Chapter 4 describes these different implementations.

2.3 Mini PCI Exceptions and Differences

Mini PCI differs from the *PCI Local Bus Specification* in the following ways:

- While the *PCI Local Bus Specification* defines 5V, 3.3V, and dual voltage add-in cards, Mini PCI supports only a 3.3V signaling environment. Therefore, there are no $V_{I/O}$ pins defined, and no connector keying. The main Vcc logic supply is 3.3V. 5V is available, but limited to 100 mA.
- Total power consumption from all sources is limited to 2.0 W.
- The 5V supply defined for Type I, II, and III Mini PCI Cards is limited to 100 mA. The VCC5VA defined for Type III only Mini PCI Cards (filtered audio 5V supply) is limited to 100 mA. The 5V and VCC5VA supply are not the same supply and cannot be connected on the Mini PCI Card. See Table 4-1 for more information regarding VCC5VA.

- 3.3VAUX is limited to 200 mA in D3 states with PME enabled and to less than 5 mA in D3 states when PME is not enabled. In D0, D1, and D2 states, it is acceptable for wake event capable Mini PCI applications to consume up to 375 mA of 3.3VAUX current.
- PCI 64-bit bus expansion is not supported.
- Maximum connector pin current capacity is 500 mA.
- +12V and -12V supplies are not implemented.
- Uninitialized (D0 uninitialized) current is limited to 70 mA rather than the 10 W afforded a standard PCI expansion card.
- Caching is not supported.
- Since a Mini PCI Card is discovered through normal **IDSEL** and configuration read sequences, the **PRESENT** pins are not required or supported. Some interrupt routing latitude, typically reserved for the system board, is allocated to the Mini PCI Card.
- Power management is required.
- The **LOCK#** signal is not supported.
- Mini PCI is 3.3V signaling only.

2.4 System Connector Pinout

The pin list in Table 2-2 shows system connector pinout for Type I and Type II cards. The pin list in Table 2-3 shows the system connector pinout for Type III cards.

Table 2-2: Mini PCI Card Type I/II System Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	INTB#	2	5V	51	SERR#	52	STOP#
3	3.3V	4	INTA#	53	GROUND	54	3.3V
5	RESERVED	6	RESERVED	55	PERR#	56	DEVSEL#
7	GROUND	8	3.3VAUX	57	C/BE[1]#	58	GROUND
9	CLK	10	RST#	59	AD[14]	60	AD[15]
11	GROUND	12	3.3V	61	GROUND	62	AD[13]
13	REQ#	14	GNT#	63	AD[12]	64	AD[11]
15	3.3V	16	GROUND	65	AD[10]	66	GROUND
17	AD[31]	18	PME#	67	GROUND	68	AD[09]
19	AD[29]	20	RESERVED	69	AD[08]	70	C/BE[0]#
21	GROUND	22	AD[30]	71	AD[07]	72	3.3V
23	AD[27]	24	3.3V	73	3.3V	74	AD[06]
25	AD[25]	26	AD[28]	75	AD[05]	76	AD[04]
27	RESERVED	28	AD[26]	77	RESERVED	78	AD[02]
29	C/BE[3]#	30	AD[24]	79	AD[03]	80	AD[00]
31	AD[23]	32	IDSEL	81	5V	82	RESERVED_WIP[2]
33	GROUND	34	GROUND	83	AD[01]	84	RESERVED_WIP[2]
35	AD[21]	36	AD[22]	85	GROUND	86	GROUND
37	AD[19]	38	AD[20]	87	AC_SYNC	88	M66EN
39	GROUND	40	PAR	89	AC_SDATA_IN	90	AC_SDATA_OUT
41	AD[17]	42	AD[18]	91	AC_BIT_CLK	92	AC_CODEC_ID0#
43	C/BE[2]#	44	AD[16]	93	AC_CODEC_ID1#	94	AC_RESET#
45	IRDY#	46	GROUND	95	MOD_AUDIO_MON	96	RESERVED
47	3.3V	48	FRAME#	97	AUDIO_GND	98	GROUND
49	CLKRUN#	50	TRDY#	99	SYS_AUDIO_OUT	100	SYS_AUDIO_IN

[2] Work in progress by the Mini PCI Working Group System Connector Sub Group.

Note that the Type III system connector is a superset of the Type I and II connectors. The signal list and layout in Table 2-3 starting at pin 17 is equivalent to pin 1 in Table 2-2. The overlapping signal region is shaded in Table 2-3.

Table 2-3: Mini PCI Card Type III System Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	TIP	2	RING	63	3.3V	64	FRAME#
	Key		Key	65	CLKRUN#	66	TRDY#
3	8PMJ-3[3, 4]	4	8PMJ-1[3, 4]	67	SERR#	68	STOP#
5	8PMJ-6[3, 4]	6	8PMJ-2[3, 4]	69	GROUND	70	3.3V
7	8PMJ-7[3, 4]	8	8PMJ-4[3, 4]	71	PERR#	72	DEVSEL#
9	8PMJ-8[3, 4]	10	8PMJ-5[3, 4]	73	C/BE[1]#	74	GROUND
11	LED1_GRNP	12	LED2_YELP	75	AD[14]	76	AD[15]
13	LED1_GRNN	14	LED2_YELN	77	GROUND	78	AD[13]
15	CHSGND	16	RESERVED	79	AD[12]	80	AD[11]
17	INTB#	18	5V	81	AD[10]	82	GROUND
19	3.3V	20	INTA#	83	GROUND	84	AD[09]
21	RESERVED	22	RESERVED	85	AD[08]	86	C/BE[0]#
23	GROUND	24	3.3VAUX	87	AD[07]	88	3.3V
25	CLK	26	RST#	89	3.3V	90	AD[06]
27	GROUND	28	3.3V	91	AD[05]	92	AD[04]
29	REQ#	30	GNT#	93	RESERVED	94	AD[02]
31	3.3V	32	GROUND	95	AD[03]	96	AD[00]
33	AD[31]	34	PME#	97	5V	98	RESERVED_WIP[5]
35	AD[29]	36	RESERVED	99	AD[01]	100	RESERVED_WIP[5]
37	GROUND	38	AD[30]	101	GROUND	102	GROUND
39	AD[27]	40	3.3V	103	AC_SYNC	104	M66EN
41	AD[25]	42	AD[28]	105	AC_SDATA_IN	106	AC_SDATA_OUT
43	RESERVED	44	AD[26]	107	AC_BIT_CLK	108	AC_CODEC_ID0#
45	C/BE[3]#	46	AD[24]	109	AC_CODEC_ID1#	110	AC_RESET#
47	AD[23]	48	IDSEL	111	MOD_AUDIO_MON	112	RESERVED
49	GROUND	50	GROUND	113	AUDIO_GND	114	GROUND
51	AD[21]	52	AD[22]	115	SYS_AUDIO_OUT	116	SYS_AUDIO_IN
53	AD[19]	54	AD[20]	117	SYS_AUDIO_OUT GND	118	SYS_AUDIO_IN GND
55	GROUND	56	PAR	119	AUDIO_GND	120	AUDIO_GND
57	AD[17]	58	AD[18]	121	RESERVED	122	MPCIACT#
59	C/BE[2]#	60	AD[16]	123	VCC5VA	124	3.3VAUX
61	IRDY#	62	GROUND				

[3] 8PMJ = 8 position modular jack connector pin, hereinafter referred to as RJ45 (see IEC 603-7:1990), see Table 2-4 for details.

[4] Note: These signals are optional and are defined to provide convenient access to LAN signals without cabling. However, due to voltage limitations of the Type III connector, additional insulation or engineering will be required to meet IEEE 802.3 and 802.5 electrical isolation requirements.

[5] Work in progress by the Mini PCI Working Group System Connector Sub Group.

2.5 Function-Specific Connectors–Communications Support

This section describes the 8 position modular jack LAN connector, hereinafter referred to as RJ45 (see IEC 603-7:1990), support for the Mini PCI Type I and Type III Cards only because Type II Cards have built in RJ connectors. Those RJ connector pinouts must be in compliance with the following specifications:

- *ISO/IEC 8802-3 ANSI IEEE Standard 802.3*
- *Supplement to ANSI/IEEE 802.3 Document 802.3u*
- *ISO/IEC 8802-5 ANSI IEEE Standard 802.5*

Table 2-4 shows Type I and Type III LAN connector pinout.

Table 2-4: Type I and Type III LAN Connector Pinout

I/O Conn	LAN Type			RJ45 (8PMJ)	Type III System Connector
Pin[6]	10 BASE-T	10-100	Token Ring	Pin	Pin[6]
1	LED1_GRNP[7]	LED1_GRNP[7]	LED1_GRNP[7]		11
2	LED1_GRNN[7]	LED1_GRNN[7]	LED1_GRNN[7]		13
3	No Connect[8]	No Connect[8]	No Connect[8]		15
4	Not used	RJ45 termination	Optionally terminated	8	9
5	Not used	RJ45 termination	Optionally terminated	7	7
6	RD-	RD-	TX+	6	5
7	Not used	RJ45 termination	RX-	5	10
8	Not used	RJ45 termination	RX+	4	8
9	RD+	RD+	TX-	3	3
10	TD-	TD-	Optionally terminated	2	6
11	TD+	TD+	Optionally terminated	1	4
12	No Connect[8]	No Connect[8]	No Connect[8]		
13	LED2_YELP[7]	LED2_YELP[7]	LED2_YELP[7]		12
14	LED2_YELN[7]	LED2_YELN[7]	LED2_YELN[7]		14

[6] Due to the high frequencies on the LAN signals, Type III implementations shall not use both an I/O connector and a system connector for LAN wiring. The Type III card and host systems supporting Type III cards must be configured for only one connector, either an I/O connector or a system connector, but not both. Using both connectors will have an adverse affect on LAN performance and reliability. Host systems shall designate which form of connection is available on the host system and only incorporate Mini PCI Cards with matching configurations. Note: The Type III system connector wiring for LAN signals is defined to provide convenient access to LAN signals without cabling. However, due to voltage limitations of the Type III connector, additional insulation or engineering will be required to meet IEEE 802.3 and 802.5 electrical isolation requirements.

[7] LED signals are optional and, if connected, are only required on the connector used for LAN signals. LED signals do not need to be wired to both the I/O Connector and the System Connector on Type III cards.

[8] This pin must be left as No Connect in order to meet IEEE 802.3 and 802.5 electrical isolation requirements.

Table 2-5 shows the pinout for the Type I and Type III modem connector.

Table 2-5: Type I and Type III Modem Connector Pinout

Pin #	Signal	Description
1	RING	RING is one conductor of the wire pair comprising the local loop.
2	TIP	TIP is one conductor of the wire pair comprising the local loop. Usually the more positive of the two conductors.

Type II modem Cards will have built-in RJ connectors whose pinouts must be in compliance with each country's regulatory agency specifications as discussed in Section 4.3.

2.5.1 LED Support

In addition to the standard LAN signal support, the Mini PCI implementation can support two LED devices in support of LAN functionality only. These LED devices can also be used in supporting LAN diagnostics which may be implementation specific. The Mini PCI Card generates and drives or sinks the LED device current as defined in Section 4.2.1. The LED device interface is supported as described in the LAN function-specific connector, as shown in Table 2-4; and optionally in the Type III system connector, as shown in Table 2-3. It is intended that one LED device be green. The second LED may be yellow, orange, or amber.

LED signals are optional and, if connected, are only required on the connector used for LAN signals. LED signals do not need to be wired to both the I/O Connector and the System Connector on Type III cards.

The LED devices are driven by the signals LEDx-yyyz where:

- x is the number 1 or 2 LED device.
- yyy indicates the color (YEL for yellow in this implementation).
- z indicates the DC polarity: N for sinking current into the pin, and P for sourcing current out of the pin.

As Table 2-4 shows, these signals then become LED1_GRNN and LED1_GRNP for the green LED device and LED2_YELN and LED2_YELP for the yellow LED device.

There is no standard convention for the implementation of LEDs for Token Ring or Ethernet. Therefore, LED functionality for the two LEDs for Token Ring and Ethernet is left undefined. Vendors are free to implement the two LEDs as they choose.

2.5.2 Chassis Ground

The signal CHSGND is a chassis ground contact and is connected on the Mini PCI Card through a mounting hole on Type I and Type II cards and via a spring contact clip on Type III cards (as illustrated in Chapter 5).

Chapter 3
Buses

3.1 Introduction

In addition to the PCI bus, Mini PCI provides for implementing several technologies which may be enumerated as buses for discussion purposes as illustrated in Figure 1-1. The buses used in a Mini PCI Card implementation consist of combinations of the following:

- The PCI local bus
- An audio bus
- A power management bus
- LAN (Ethernet and Token Ring) buses
- A modem bus

Existing specifications define the implementations of these functional buses.

3.2 System Connector

Table 3-1 summarizes the appropriate specifications regarding the buses implemented in the Mini PCI Card system connector.

Table 3-1: System Connector Specifications

Signals	Bus Implementation	Governing Specification
INTA#, **INTB#**, **C/BE[0::3]#**, **STOP#**, **DEVSEL#**, **IDSEL**, **CLK**, **RST#**, **AD[00::31]**, **REQ#**, **GNT#**, **PAR**, **PERR#**, **SERR#**, **M66EN**, **IRDY#**, **TRDY#**, **FRAME#**	PCI	*PCI Local Bus Specification*, Chapter 3
PME#, **3.3VAUX**	Power management	*PCI Bus Power Management Interface Specification*
CLKRUN#	Power management	*PCI Mobile Design Guide*
AC_SYNC, AC_SDATA_IN, AC_SDATA_OUT, AC_BIT_CLK, AC_CODEC_ID0#, AC_CODEC_ID1#, AC_RESET#	AC-link support	*Audio Codec '97 Component Specification*
MOD_AUDIO_MON, SYS_AUDIO_OUT, SYS_AUDIO_IN, SYS_AUDIO_OUT_GND[9] SYS_AUDIO_IN_GND[9] AUDIO_GND	System audio	These audio signals are implementation specific. Refer to Chapter 4 of this specification for characteristics.
TIP[9], RING[9]	Modem	Specific to country's regulatory agency specifications
8PMJ1-8[9,10]	LAN	Refer to Table 3-2 for governing specifications

[9] Available on the system connector in the Type III form factor only.

[10] Note: These signals are optional and are defined to provide convenient access to LAN signals without cabling. However, due to voltage limitations of the Type III connector, additional insulation or engineering will be required to meet IEEE 802.3 and 802.5 electrical isolation requirements.

3.3 Function-Specific Connector

Table 3-2 summarizes the appropriate specifications regarding the buses implemented in the Mini PCI Card function-specific connector.

Table 3-2: Function-Specific Connector Specifications

Signals	Bus Implementation	Governing Specification
RD-, RD+, TD-, TD+	Ethernet	*ISO/IEC 8802-3 ANSI IEEE Standard 802.3 Supplement to ANSI/IEEE 802.3 Document 802.3u*
TX-, TX+, RX-, RX+	Token Ring	*ISO/IEC 8802-5 ANSI IEEE Standard 802.5*
TIP, RING	Modem	Specific to country's regulatory agency specifications
LED1_GRNP, LED1_GRNN, LED2_YELP, LED2_YELN	Local area network support	Implementation specific
RJ45 termination	Local area network support	Technology specific

Chapter 4
Electrical Specification

4.1 System Interface Connector

The electrical characteristics of each bus specified in this specification are implemented according to the relevant bus specification as shown in Table 4-1.

An exception exists for Mini PCI with regard to the implementation of the PCI bus **CLK** signal. The *PCI Local Bus Specification* requires that the **CLK** signal be 2.5 inches in length on the PCI card. This length is reduced to 25.4 mm ±2.5 mm (1.0 inch ±0.1 inches) for the Mini PCI Card and must be routed to only one load. This deviation from the *PCI Local Bus Specification* requires that the system board design be responsible for clock/data timing. All other characteristics of the **CLK** signal are as defined in the *PCI Local Bus Specification*.

Table 4-1: System Connector Specifications

System Connector		
Signals	**Bus Implementation**	**Governing Specification**
INTA#, **INTB#**, **C/BE[0::3]#**, **STOP#**, **DEVSEL#**, **IDSEL**, **CLK**, **RST#**, **AD[00::31]**, **REQ#**, **GNT#**, **PAR**, **PERR#**, **SERR#**, **M66EN**, **IRDY#**, **TRDY#**, **FRAME#**	PCI	*PCI Local Bus Specification*, Chapter 4
PME#, **3.3VAUX**	Power management	*PCI Bus Power Management Interface Specificiation*
CLKRUN#	Power management	*PCI Mobile Design Guide*
MPCIACT#	Power management and general purpose	Refer to Section 4.5 for more information.
AC_SYNC, AC_SDATA_IN, AC_SDATA_OUT, AC_BIT_CLK, AC_ CODEC_ID0#, AC_CODEC_ID1#, AC_RESET#	AC-link support	*Audio Codec '97 Component Specification*

Table 4-1: System Connector Specifications (continued)

System Connector		
Signals	**Bus Implementation**	**Governing Specification**
TIP[11], RING[11]	Modem	Specific to country's regulatory agency specifications. Refer to Section 4.1.1 for specific wiring ground rules.
8PMJ1-8[11], [12]	LAN	Refer to Table 4-2 for governing specifications

System Audio

System Audio Signal	Voltage Range	Impedance	Test Conditions
SYS_AUDIO_OUT	700 mV RMS Nominal 1000 mV RMS Max	Mini PCI Card termination impedance: 50 kΩ minimum System source impedance: 600 Ω, maximum	300 Hz-3.4 kHz ±1 dB
SYS_AUDIO_IN	700 mV RMS Nominal 1000 mV RMS Max	Mini PCI Card source impedance: 600 Ω, maximum System termination impedance: 50 kΩ, minimum	300 Hz-3.4 kHz ±1 dB
MOD_AUDIO_MON	Refer to the *PC Card Electrical Specification*, Section 5.2.12 for specification of the electrical characteristics of this signal		
AUDIO_GND	Connected to system board audio ground		
SYS_AUDIO_OUT_GND[11]	Return signal for SYS_AUDIO_OUT. This may be used as a ground or may be used as a return for differentially receiving SYS_AUDIO_OUT. See Figure 4-1.		
SYS_AUDIO_IN_GND[11]	Return signal for SYS_AUDIO_IN. This may be used as a ground or may be used as a return for differentially receiving SYS_AUDIO_IN. See Figure 4-1.		
VCC5VA[11]	5 Volts ±5%, 100 mA maximum. Used primarily for voice circuit on modem card but may be used where quiet analog supply is needed. Voltage is supplied by system board to Type III Mini PCI Card. VCC5VA power return signal is AUDIO_GND.		

[11] Available on the system connector in the Type III form factor only.

[12] Note: These signals are optional and are defined to provide convenient access to LAN signals without cabling. However, due to voltage limitations of the Type III connector, additional insulation or engineering will be required to meet IEEE 802.3 and 802.5 electrical isolation requirements.

4.1.1 Audio Interface Modes

Three interconnect options are provided for the analog audio interface signals. The signals may be connected in a single-ended fashion as shown in Figure 4-1 for all cards; or, as in Figure 4-2 for Type III cards only. The signals may also be connected in a quasi-differential fashion as shown in Figure 4-2 for Type III cards only. The implementation permits any combination of single-ended/differential system/Mini PCI Card configurations.

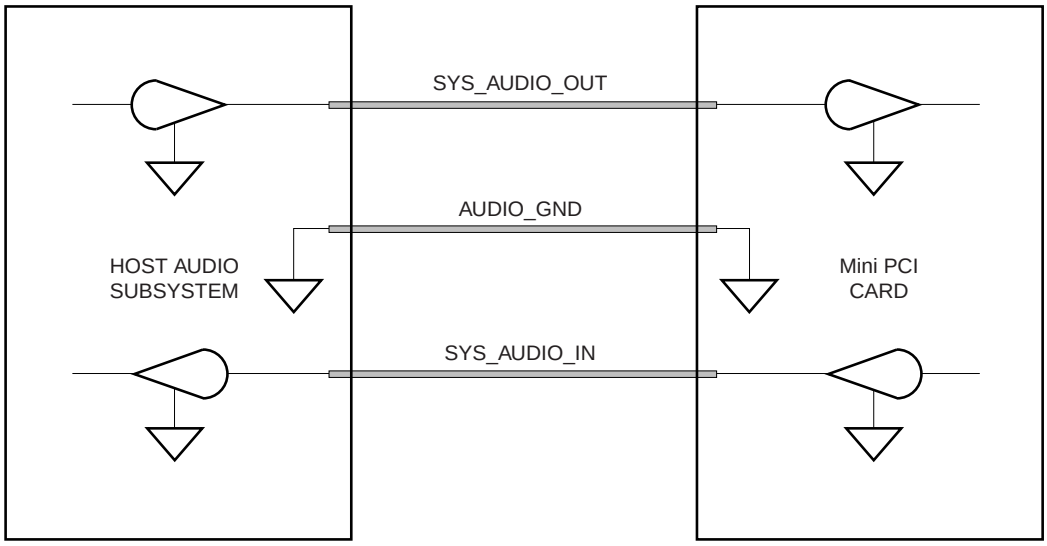


Figure 4-1: System Audio Implementation for All Types

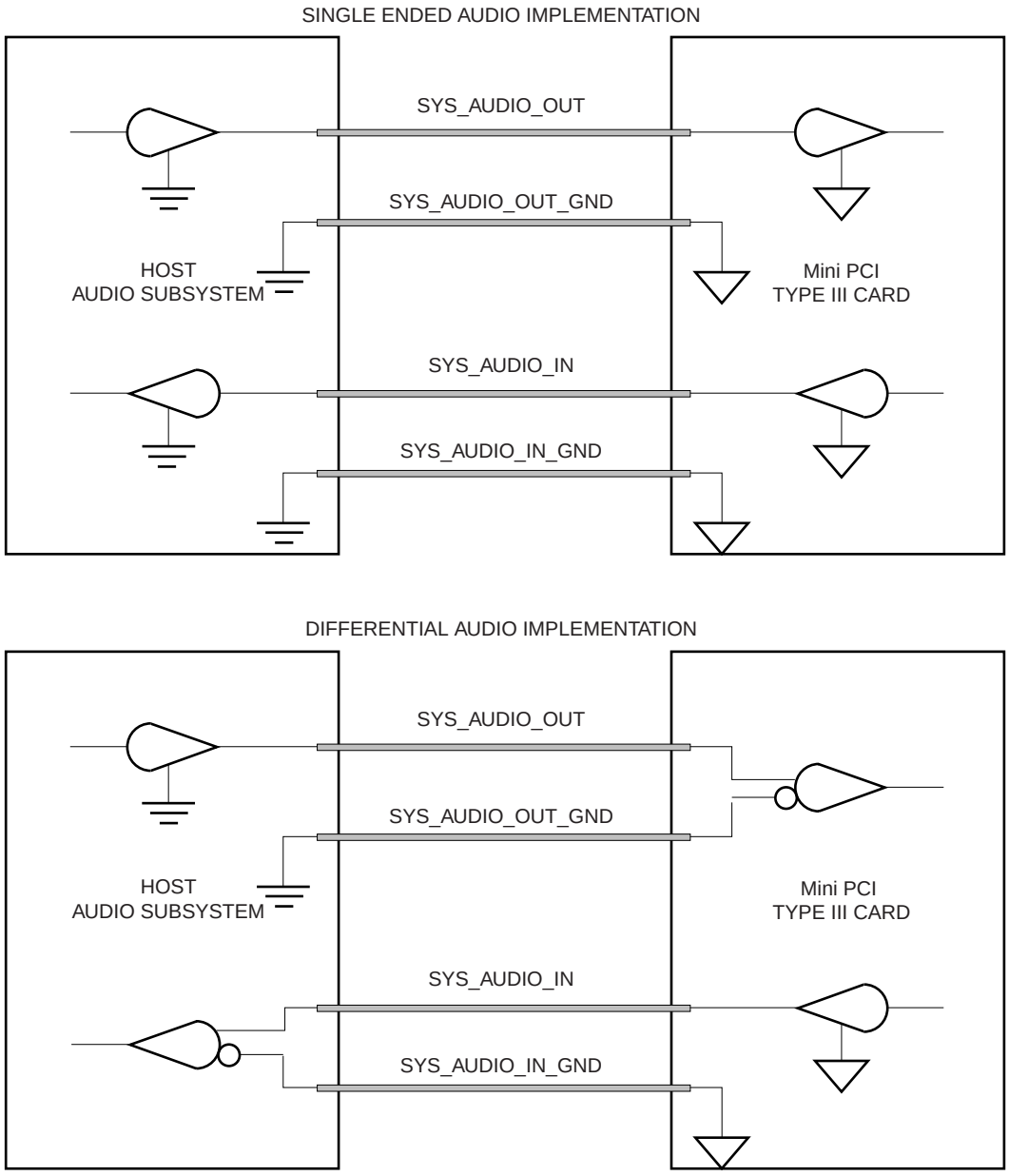


Figure 4-2: Example of Single Ended and Differential Audio Signals for Type III Only

4.2 Mini PCI Function-Specific Connector

The functional buses of Mini PCI consist of local area network support for Ethernet and Token Ring implementations, LED indicator support, and modem support. Table 4-2 lists the specifications governing the operation of these buses.

Table 4-2: Function-Specific Connector Specifications

Signals	Bus Implementation	Governing Specification
RD-, RD+, TD-, TD+	Ethernet	*ISO/IEC 8802-3 ANSI IEEE Standard 802.3* *ANSI/IEEE 802.3 Document 802.3u*
TX-, TX+, RX-, RX+	Token Ring	*ISO/IEC 8802-5 ANSI IEEE Standard 802.5*
TIP, RING	Modem	
LED1_GRNP, LED1_GRNN, LED2_YELP, LED2_YELN	Local area network support	As described in Section 2.5.1 of this specification
RJ45 termination	Local area network support	Technology specific

4.2.1 LED Voltage and Current Specifications

LED1_GRNP and LED2_YELP output signals are intended to provide a current limited supply voltage to system-mounted LED indicators. These signals shall provide one of the following:

- 5 V ±5% through a series resistance of 422 ohms ±1%
- 3.3 V ±5% through a series resistance of 187 ohms ±1%

LED1_GRNN and LED2_YELN output signals are active low and are intended to drive system-mounted LED indicators. These signals shall be capable of sinking to ground a minimum of 9.0 mA.

The specifications listed in Table 4-2 provide approximately 7.0 mA of LED current assuming a typical forward voltage for the LED of Vf(typ) = +2.0 V dc.

4.3 Communications Signal Characteristics and EMC

Mini PCI Cards shall be tested and certified to the applicable standards for telecommunications devices per each country's regulations. Some examples of regulatory standards writing bodies and applicable standards are:

- ACA – Australian Communications Authority (Australia) TS 002 and TS 004
- IC – Industry Canada (Canada) CS-03 Issue 8 and IEES-003
- JATE – Japan Authority for Telecommunications Equipment (Japan) Blue Book
- FCC – Federal Communications Commission (United States of America) 47 CFR Parts 15 and 68
- CTR21 – Common Technical Regulation 21
- CENELEC – European Committee for Standards – Electrical (European) EN55022 and EN50082-1
- IEC – International Electrotechnical Commission(International) CISPR 22

- VCCI – Voluntary Control Council for Interference by Information Technology Equipment

It is the host system manufacturer's responsibility to ensure that the complete system/card combination complies with the applicable country's regulations.

4.3.1 Modem

Mini PCI Cards shall comply with the electromagnetic compatibility (EMC) requirements applicable per each country's regulations. Country specific requirements may include limits on Out of Band Noise (lower frequency emissions near the transmitted signal band), radiated and conducted emissions, immunity and susceptibility.

4.3.2 NIC

As with modems, Mini PCI Card NICs shall comply with the electromagnetic compatibility (EMC) requirements applicable per each country's regulations.

4.3.3 Host System

Host systems designed to receive Mini PCI Cards shall comply with the EMC requirements per each country's regulations in relation to the I/O signals. Country specific requirements may include limits on Out of Band Noise (lower frequency emissions near the transmitted signal band), radiated and conducted emissions, immunity and susceptibility.

The I/O modem cable itself can degrade the Out of Band Noise performance if proper care is not exercised in the routing path within the system. The physical proximity of the cable to certain high frequency and high current switching elements (such as the microprocessor) can significantly affect results. As a general rule, the cable should be kept as short as possible and should be routed in such a way as to minimize its proximity to the high radiation sources within the system. If shielding becomes necessary, make sure the shield does not violate the TNV insulation and isolation requirements. The host system manufacturer shall ensure that the fully assembled system, including the modem and cable, complies with the Out of Band Noise emissions and Electromagnetic Compatibility requirements. Compliance should be confirmed by measuring the emissions level with respect to the particular national requirements of the receiving country.

System designers should take care to minimize the possibility of electromagnetic interference (EMI) coupling onto the Tip and Ring signals. This should include careful consideration in the frequency range from 4 kHz to 10 MHz, where additional noise coupled to the signal path may impair the modem's ability to comply with the type approval requirements.

As with the Out of Band Noise, EMI performance can be degraded by the cable. This can be caused by energy induced into the cable from circuit elements which are in close proximity as well as energy from the Mini PCI Card itself. The same guidelines outlined for the Out of Band Noise applies to minimizing EMI. Compliance should be confirmed by measuring the emissions level with respect to the particular national requirements of the receiving country.

NIC performance can be severely impacted by EMI coupled onto the signal paths. It is recommended that the signal paths be designed to meet the electrical attributes described in EIA/TIA 568-A and TSB-36 for Category 5 cabling.

NIC cable shielding shall be optional and is determined based on the individual system requirements. For systems with relatively long cables, it may become necessary to shield the cable in order to meet EMI requirements. The presence of a shield can affect the impedance and return loss of the cable and, therefore, shall be factored into the overall cable design. It is recommended that the shield be connected to the chassis ground of the system.

4.3.4 Labeling

In cases where the Mini PCI Card is not user accessible, approval labels for the card may need to appear on the host platform with a note on the label stating that the approvals apply to the card and not the host system. The card may also be required to bear some safety, telecom, and EMC approval markings depending on the requirements of the receiving country. It is the responsibility of the host system manufacturer to ensure that the labeling is affixed in accordance with local regulations.

4.3.5 NIC Performance Considerations

NIC performance can be severely impacted by the design of the signal paths. Whether the NIC signals are routed through the host system board or a cable, one of the most important NIC performance considerations is the characteristic impedance of the conductors. If the conductor impedance does not closely match that of the Telecommunications Outlet (TO) and onboard PHY, reflections will occur which can cause significant performance reduction. Under severe mismatch conditions, complete loss of connectivity can occur. A properly designed transmission path should present an impedance of 100 ohms, ±15% in the frequency range 1 MHz to 100 MHz. The signal path construction is critical to controlling this impedance.

A NIC cable may be constructed in many different ways but, as a general rule, the cable should meet the electrical attributes described in EIA/TIA 568-A and TSB-36 for Category 5 cabling. In the case of a twisted pair cable, the wire gauge, insulation, and twist parameters affect the cable impedance. With flex cable construction, the strip line constants such as trace width, trace spacing, and dielectric thickness control the cable impedance.

Insertion loss of the NIC signal path including connectors should be equal to or better than an equivalent length of Category 5 cable. Refer to EIA/TIA 568-A Section 10.5. Refer to EIA/TIA 568-A Annex B, ANSI/IEEE 802.3 and ANSI X3.263 1995 clause 11 for more details on methods and techniques for measuring this parameter.

Crosstalk is an unwanted signal coupled, either capacitively or inductively, from one signal path to another. The NIC signal path should be designed to minimize crosstalk. Refer to EIA/TIA 568-A and ANSI X3.263 1995 for crosstalk requirements and test methods.

Although termination of the unused NIC pairs is implementation specific, it is recommended that they be terminated. The purpose of termination is to reduce the noise and crosstalk coupled from the unused pairs onto the used pairs. Methods for termination include:

- 100 ohm resistor placed across the pair and left floating
- RC network from each conductor to ground
- RC network from each conductor to a termination plane

It is recommended that the use of stubs (un-terminated lengths of signal path) be avoided. Stubs cause signals to be reflected back from the far end of the stub and can cause a significant reduction in NIC performance. A stub cannot be properly terminated without excessively attenuating the output signal.

The presence of a shield around the NIC signals can affect the impedance and return loss of the signal path and, therefore, shall be factored into the overall signal path design. It is recommended that the shield be connected to the chassis ground of the system.

The NIC signal paths are part of the network adapter interface and can impact network performance. Therefore, NIC performance should be verified to be compliant with characteristics and templates described in ANSI X3.263 1995 clause 9 (and those clauses of ANSI/IEEE 802.3 that are appropriate for the technologies supported by the Mini PCI NIC) when installed in the host system.

4.4 PCI Bus Loading

The PCI bus loading is defined in the *PCI Local Bus Specification.*

4.5 MPCIACT# Signal

MPCIACT#, Mini PCI function active, is intended to indicate, when low, that the Mini PCI Card is in a communicating state requiring full system performance. This signal is optional for systems and shall be used to prevent system suspend and limit CPU clock throttling where necessary.

MPCIACT# is required for all Mini PCI Cards implementing functions that have critical system performance requirements, such as a software modem, or that have critical times where the Mini PCI function cannot tolerate system suspend. This signal should be active whenever the PCI function requires maximum system performance, or requires that the system not enter any suspended state. Typically, a modem would activate this signal when the modem is in an off hook state. This signal is not necessary for Mini PCI Cards where means to guarantee maximum system performance are either unnecessary or are provided through some other means.

This signal is an open drain/collector signal with a V_{ol} max of 0.8V with an I_{ol} max of 5 mA.

The Mini PCI Card shall be tolerant of 5V pullup on this pin. The Mini PCI Card may use a pullup on this pin as long as the V_{ol} max at I_{ol} max is maintained and the pullup is tied to 3.3V. The pullup shall not be tied to 3.3VAUX or 5V. The system board may pull this signal to 3.3V or 5V as required as long as the pullup resistance is greater than V/5 mA.

The Mini PCI Card shall not source more than 10 µA from MPCIACT# in the suspended state (3.3V and 5V are off). The maximum leakage current into this output, when not asserted (high state), shall be 40 µA. The leakage current shall be measured with the output tied to +5.5Vdc over the full temperature range of the Mini PCI Card.

Chapter 5
Mechanical Specification

5.1 Overview

This specification was created to define Mini PCI Cards for systems in which a standard PCI expansion card cannot be used due to mechanical system design constraints. The specification defines three form factors: Type I and Type II are single 100-pin connector interfaces; Type III is a single 124-pin connector interface. The Type I and Type II Mini PCI Cards use one miniature stacking connector. The Type III Mini PCI Card uses a card-edge type connector similar to the SO-DIMM type.

5.2 Safety

The specifications governing the mechanical and electrical safety requirements (for example, creepage and clearance requirements) for modem and network interface cards may include those in Table 5-1.

Table 5-1: Function-Specific Connector Specifications

Bus Implementation	Governing Specifications
Ethernet	*ISO/IEC 8802-3 ANSI IEEE Standard 802.3* *Supplement to ANSI/IEEE 802.3 Document 802.3u*
Token Ring	*ISO/IEC 8802-5 ANSI IEEE Standard 802.5*
Modem	Specific to country's regulatory agency specifications

Mini PCI Cards shall be tested and certified to comply with the applicable international safety standards for telecommunications devices per each country's regulations. Some examples of regulatory standards writing bodies and applicable standards are:

- CSA – Canadian Standards Association (Canada) CAN/CSA C22.2 No. 950
- CENELEC – European Committee for Standards – Electrical (European) EN 60950
- IEC – International Electrotechnical Commission (International) IEC60950
- JATE – Japan Authority for Telecommunications Equipment (Japan) Blue Book
- UL – Underwriters Laboratories, Inc. (United States of America) UL 1950

Note: It is the Mini PCI Card manufacturer's responsibility to ensure that the Mini PCI Card complies with the applicable country's current regulations. It is the host system manufacturer's responsibility to ensure that the complete system/card combination complies with the applicable country's current regulations.

5.2.1 Modem Safety

Mini PCI Cards shall comply with the safety requirements applicable per each country's regulations. Some examples of safety specifications are IEC60950, UL1950 / CSA C22.2 No. 950, and EN60950. The Mini PCI Card shall provide, within the Mini PCI Card form factor envelope dimensions defined in this chapter, sufficient electrical insulation to meet all applicable insulation and spacing (creepage/clearance distance) requirements when the Mini PCI Card is installed in the host system. Insulation and spacing requirements may include:

- 2.0 mm clearance and 2.5 mm creepage between Telecom Network Voltage (TNV) circuitry and ground.
- A single layer of insulation between TNV and ground of at least 0.4 mm thick.
- Two layers of insulation between TNV and ground, each layer being able to withstand 1500 VAC dielectric voltage. (A six-week temperature cycling test and 100% dielectric test may also be required unless a 2.0 mm clearance and 2.5 mm creepage distance is maintained between TNV circuitry and the edge of the insulation.)
- Three or more layers of insulation separating TNV from ground, each combination of two layers being able to withstand 1500 VAC dielectric voltage (A six-week temperature cycling test and 100% dielectric test may also be required unless a 2.0 mm clearance and 2.5 mm creepage distance is maintained between TNV circuitry and the edge of the insulation.)

A specific area of concern is the spacing (creepage/clearance distance) at the seams or openings in the card insulator. Also, care should be taken to ensure that the fit of the card in the host allows for sufficient spacing to other components in the system. Reduced spacing to the card insulator may increase the risk of compromising the insulator integrity.

If a Mini PCI Card is intended to be sold into a country that requires (via NRTL) UL1950 /CSA C22.2 No. 950, TNV protection against overvoltage, a means for the Mini PCI Card to comply shall be provided on the Mini PCI Card itself. The Mini PCI Card may need to include one or more of the following for compliance:

- A fusible link to prevent damage and flame
- A flame enclosure
- An external line cord with a minimum conductor size of 26 AWG
- Warnings or special instructions in the user information

5.2.2 NIC Safety

For combination network adapter/modem cards, the NIC signals shall be considered equipment voltage and shall be separated or insulated from the modem TNV circuitry.

The accidental insertion of the RJ11 telephone cable into the NIC's 8-pole modular connector is also a potential safety concern. It is recommended the system manufacturer provide a cautionary label discouraging the connection of a TNV RJ11 into the NIC's RJ45 connector. It is also recommended the NIC manufacturer test for conformance with IEC 60950 and other applicable standards in the event of a connector mismatch fault condition.

5.2.3 I/O Connector Safety

Where an RJ11 I/O connector is required, it is recommended that it:

- Comply with the dimensions and physical characteristics as specified in Part 68, Subpart F of the FCC rules and Industry Canada - CS-03, Part III
- Be a UL Listed or UL Recognized Communication Circuit Accessory
- Be CSA Certified in accordance with CSA C22.2 No. 182.4
- Comply with the requirements of UL1950/CSA C22.2 No. 950

Where an RJ45 I/O connector is required, it is recommended that it:

- Comply with the dimensions and physical characteristics as specified in ISO/IEC 8877
- Be a UL Listed or UL Recognized Communication Circuit Accessory
- Be CSA Certified in accordance with CSA C22.2 No. 182.4
- Comply with the requirements of UL1950 /CSA C22.2 No. 950

Where a 2-position or 14-position I/O connector is required, it is recommended that it:

- Be a UL Listed or UL Recognized Communication Circuit Accessory
- Be molded of plastics rated UL 94V-2 or less flammable when tested to UL 94
- Be CSA Certified in accordance with CSA C22.2 No. 182.4
- Comply with the requirements of UL1950 /CSA C22.2 No. 950

5.2.4 Host System Safety

Host systems designed to receive a Mini PCI Card shall comply with the safety requirements per each country's regulations in relation to the Tip and Ring signal paths. This is to assist in achieving regulatory agency approval of the Mini PCI Card independent of the host system.

Mini PCI Card modem Tip and Ring signals shall be classified as TNV and, as such, shall comply with all applicable country regulations.

Spacing and isolation between Tip and Ring signals and all other non-TNV signals (including power and ground planes) shall be kept great enough to pass each country's safety regulations.

The internal Tip and Ring conductors that connect the Mini PCI Card to the RJ11 on the outside of the host system shall be of a "pass through" design with no series filtering elements and no added components which could affect the Mini PCI approval status. A

simple cable with only a connector at each end is the most straightforward approach to meet this requirement.

The internal Tip and Ring conductors shall comply with the applicable regulatory requirements in the countries where the cable is intended for use. Some requirements may be included in FCC Part 68, CS-03 Part 1 and UL1950 / CSA C22.2 No. 950. Tip and Ring signal conductors shall withstand surge and over-voltage currents defined in each country's safety regulations. This implies that the appropriate cable and trace size and cable and trace material shall be selected to ensure this compliance. The conductors shall be appropriately sized to avoid excessive heating under fault conditions and to ensure that no safety hazard is presented. It is recommended that internal Tip and Ring conductors have a cross-section equal to or greater than 26 AWG. Smaller conductors may be used. Testing should always be done to ensure product safety and compliance. If testing is required, the internal Tip and Ring conductors shall be tested as part of the overall host system.

5.2.5 Labeling

In cases where the Mini PCI Card is not user accessible, approval labels for the Mini PCI Card may need to appear on the host platform with a note on the label stating that the approvals apply to the Mini PCI Card and not the host system. The Mini PCI Card may also be required to bear some safety, telecom, and EMC approval markings depending on the requirements of the receiving country. It is the responsibility of the host system manufacturer to ensure that the labeling is affixed in accordance with local regulations.

5.3 Physical Configuration

There are two basic Mini PCI Card physical configurations. The Type I/Type III Mini PCI Card is intended to support cards not placed at the outer edge of the host system (Figure 5-1). I/O connectors are mated to the Type I and Type III Mini PCI Card by a cable and header scheme.

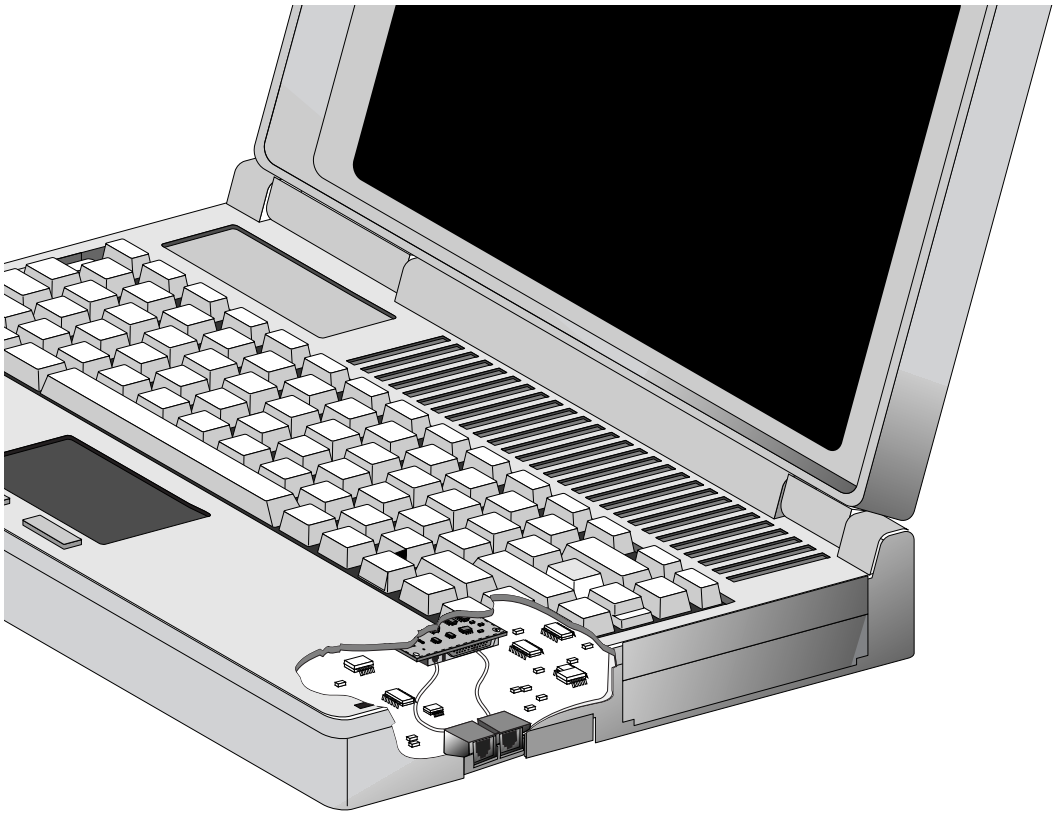


Figure 5-1: Type I or Type III Mini PCI Card (Sample Installation)

The Type II Mini PCI Card is intended to support cards placed at the outer edge of the host system. The RJ11 and RJ45 connectors are placed directly on the Mini PCI Card as shown in Figure 5-2.

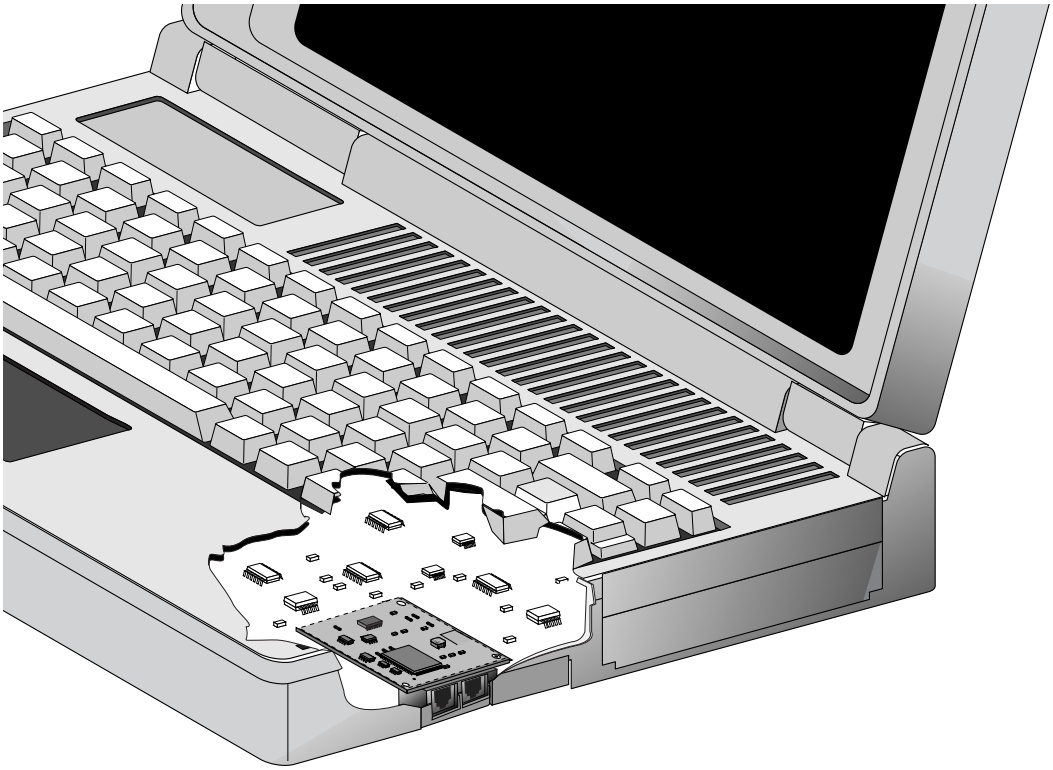


Figure 5-2: Type II Mini PCI Card (Sample Installation)

The Type III Mini PCI Card is intended for very thin profile designs. The Type III card is similar to the Type I card in that I/O connectors may be mated to a cable and header scheme. Because of the Type III's larger pin count and voltage isolation key, designers may choose to connect to modem interfaces via the system connector and system board wiring. See Figure 5-1 for a sample installation.

5.4 Mechanical Design Details

This section includes mechanical design details for each type of card. The figures in this section illustrate the form factors for each type of card. The "A" and "B" suffixes designate a difference in the size of each assembly. The alternate I/O connector region in each form factor is a designated location for any I/O connector other than those defined in this specification. Acceptable alternate I/O connectors include cellular or ISDN connectors, for example.

5.4.1 Type IA Form Factor

The Type IA form factor supports a card that is not placed at the outer edge of the host system. The form factor for Type IA differs from that of Type IB in that Type IA has a greater Z dimension or height. The form factor for Type IA is further characterized by the following guidelines:

- All dimensions are in millimeters, unless otherwise specified.
- All dimension tolerances are ±.25 mm, unless otherwise specified.
- Dimensions marked with an asterisk (*) are overall envelope dimensions and include space allowances for insulation to comply with regulatory and safety requirements.
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads.
- Although Figure 5-3 illustrates a Type IA configuration with both a modem and a LAN connector, acceptable configurations are for modem only, LAN only, and LAN and modem combinations (as shown). The location of each connector remains the same for each configuration.
- The Alternate I/O Connector Region is space on the Mini PCI Card that is designated for the location of any alternate or auxiliary I/O connectors. If no alternate or auxiliary connectors are required on a design, then the space can be used for standard component placement.

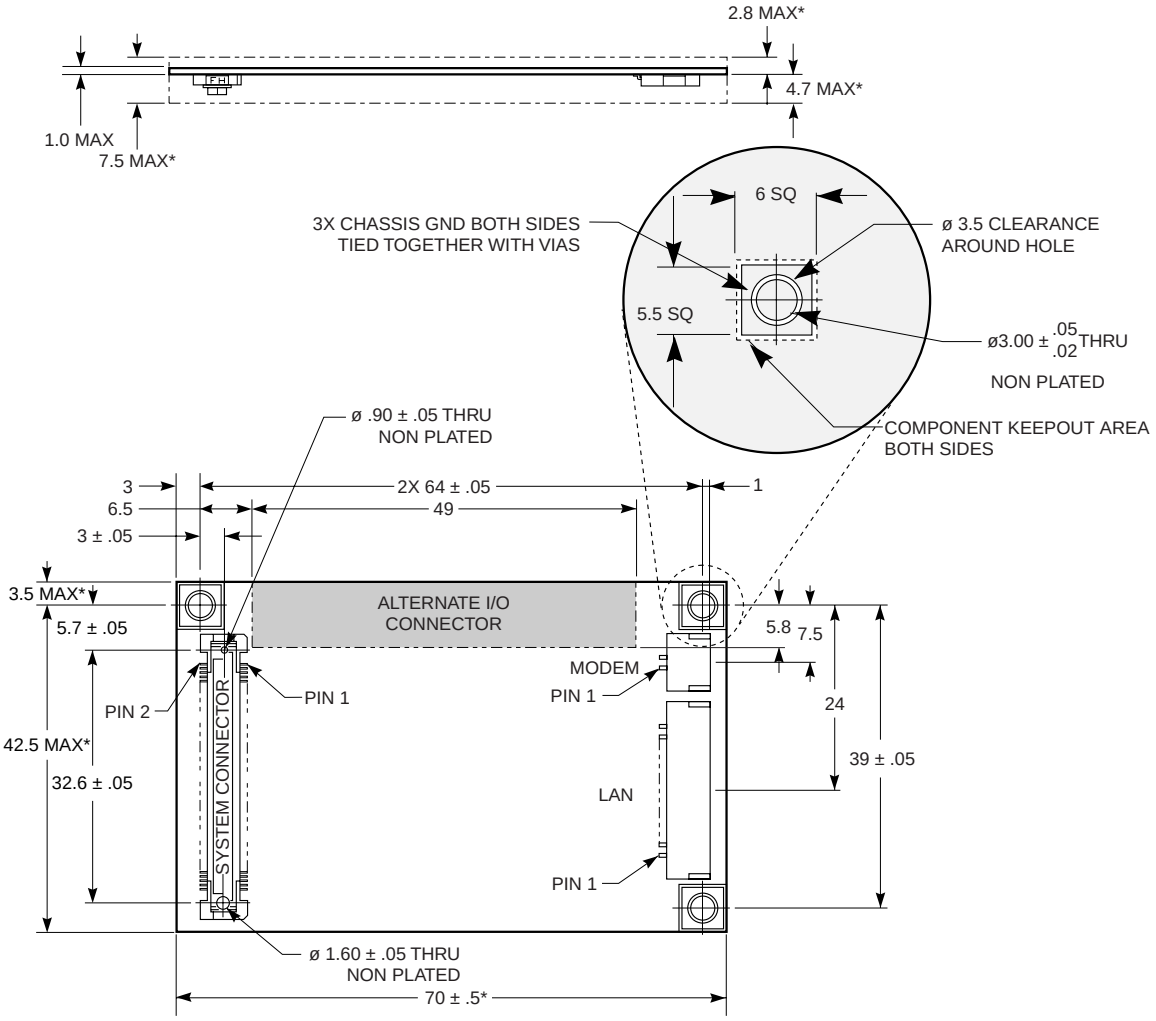


Figure 5-3: Type IA Form Factor

5.4.2 Type IB Form Factor

The Type IB form factor supports a card that is not placed at the outer edge of the host system. The form factor for Type IB differs from that of Type IA in that Type IB has a smaller Z dimension or height. The form factor for Type IB is further characterized by the following guidelines:

- All dimensions are in millimeters, unless otherwise specified.
- All dimension tolerances are ±.25 mm, unless otherwise specified.
- Dimensions marked with an asterisk (*) are overall envelope dimensions and include space allowances for insulation to comply with regulatory and safety requirements.
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads.
- Although Figure 5-4 illustrates a Type IB configuration with both a modem and a LAN connector, acceptable configurations are for modem only, LAN only, and LAN and modem combinations (as shown). The location of each connector remains the same for each configuration.
- The Alternate I/O Connector Region is space on the Mini PCI Card that is designated for the location of any alternate or auxiliary I/O connectors. If no alternate or auxiliary connectors are required on a design, then the space can be used for standard component placement.

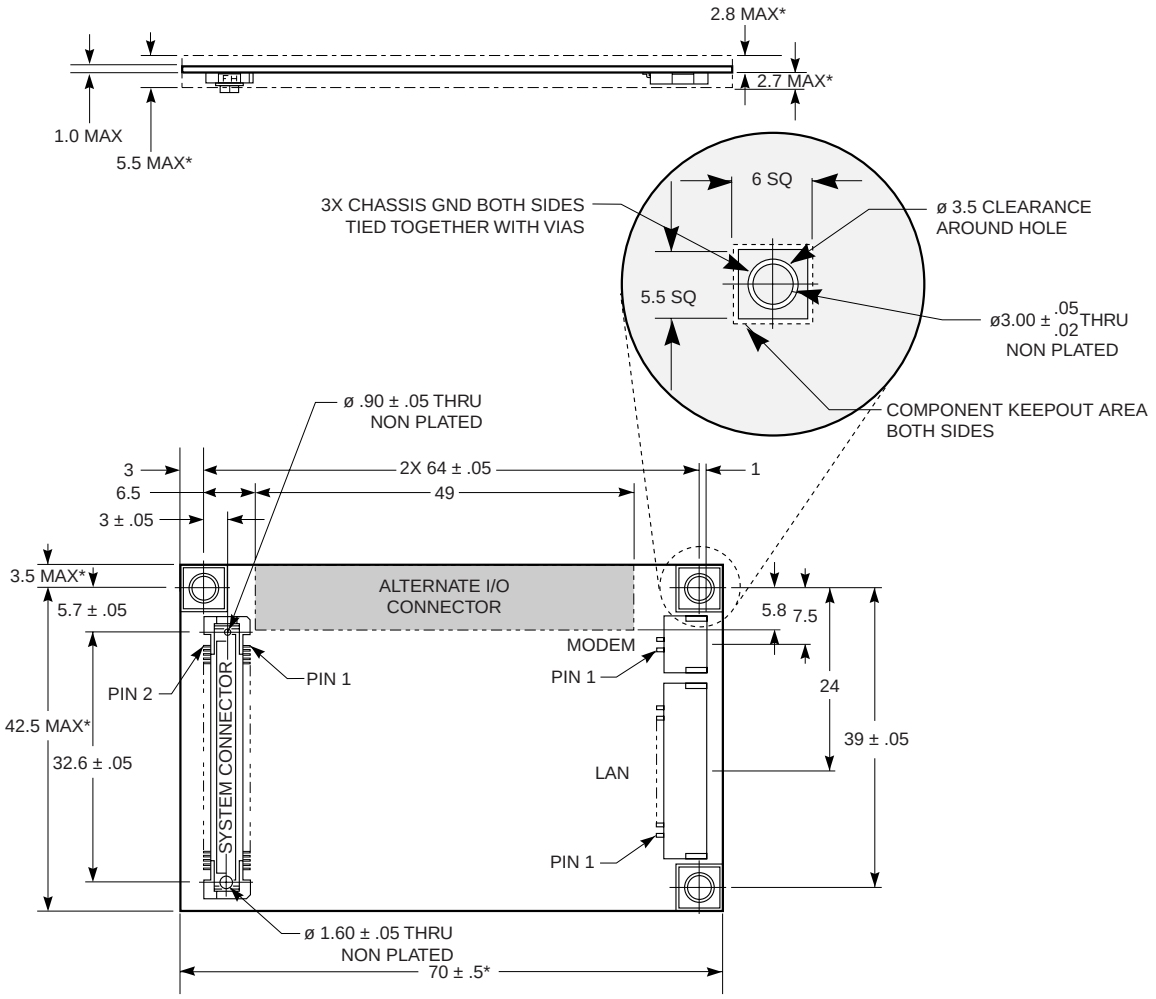


Figure 5-4: Type IB Form Factor

5.4.3 Type IIA Form Factor

The Type IIA form factor supports a card that is placed at the outer edge of the host system. The form factor for Type IIA differs from that of Type IIB in that Type IIA has a greater Z dimension or height. The form factor for Type IIA is further characterized by the following guidelines:

- All dimensions are in millimeters, unless otherwise specified.
- All dimension tolerances are ±.25 mm, unless otherwise specified.
- Dimensions marked with an asterisk (*) are overall envelope dimensions and include space allowances for insulation to comply with regulatory and safety requirements.
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads.
- Although Figure 5-5 illustrates a Type IIA configuration with both a modem and a LAN connector, acceptable configurations are for modem only (RJ11 only), LAN only (RJ45 only), and LAN and modem combinations (both RJ11 and RJ45 populated as shown). The location of each connector remains the same for each configuration. When designing a Type II Mini PCI Card with a single external I/O connector, the unpopulated connector volume, the surface of which is defined vertically by the Mini PCI Card printed circuit board outline, is owned by the Mini PCI Card. The unpopulated connector volume that is outside the defined vertical surface is owned by the host system manufacturer.
- The Alternate I/O Connector Region is space on the Mini PCI Card that is designated for the location of any alternate or auxiliary I/O connectors. If no alternate or auxiliary connectors are required on a design, then the space can be used for standard component placement.

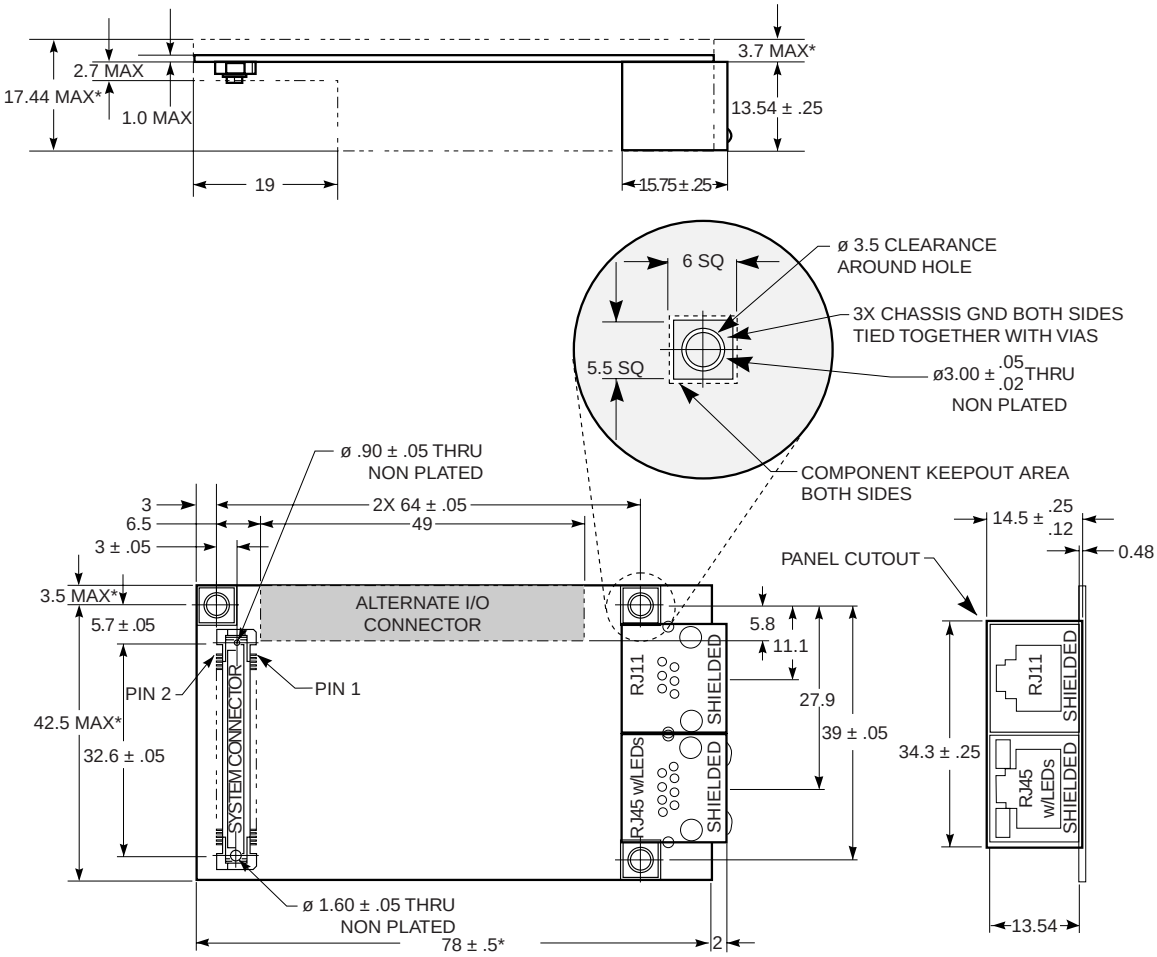


Figure 5-5: Type IIA Form Factor

5.4.4 Type IIB Form Factor

The Type IIB form factor supports a card that is placed at the outer edge of the host system. The form factor for Type IIB differs from that of Type IIA in that Type IIB has a smaller Z dimension or height. The form factor for Type IIB is further characterized by the following guidelines:

- All dimensions are in millimeters, unless otherwise specified.
- All dimension tolerances are ±.25 mm, unless otherwise specified.
- Dimensions marked with an asterisk (*) are overall envelope dimensions and include space allowances for insulation to comply with regulatory and safety requirements.
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads.
- Although Figure 5-6 illustrates a Type IIB configuration with both a modem and a LAN connector, acceptable configurations are for modem only (RJ11 only), LAN only (RJ45 only), and LAN and modem combinations (both RJ11 and RJ45 populated as shown). The location of each connector remains the same for each configuration. When designing a Type II Mini PCI Card with a single external I/O connector, the unpopulated connector volume, the surface of which is defined vertically by the Mini PCI Card printed circuit board outline, is owned by the Mini PCI Card. The unpopulated connector volume that is outside the defined vertical surface is owned by the host system manufacturer.
- The Alternate I/O Connector Region is space on the Mini PCI Card that is designated for the location of any alternate or auxiliary I/O connectors. If no alternate or auxiliary connectors are required on a design, then the space can be used for standard component placement.

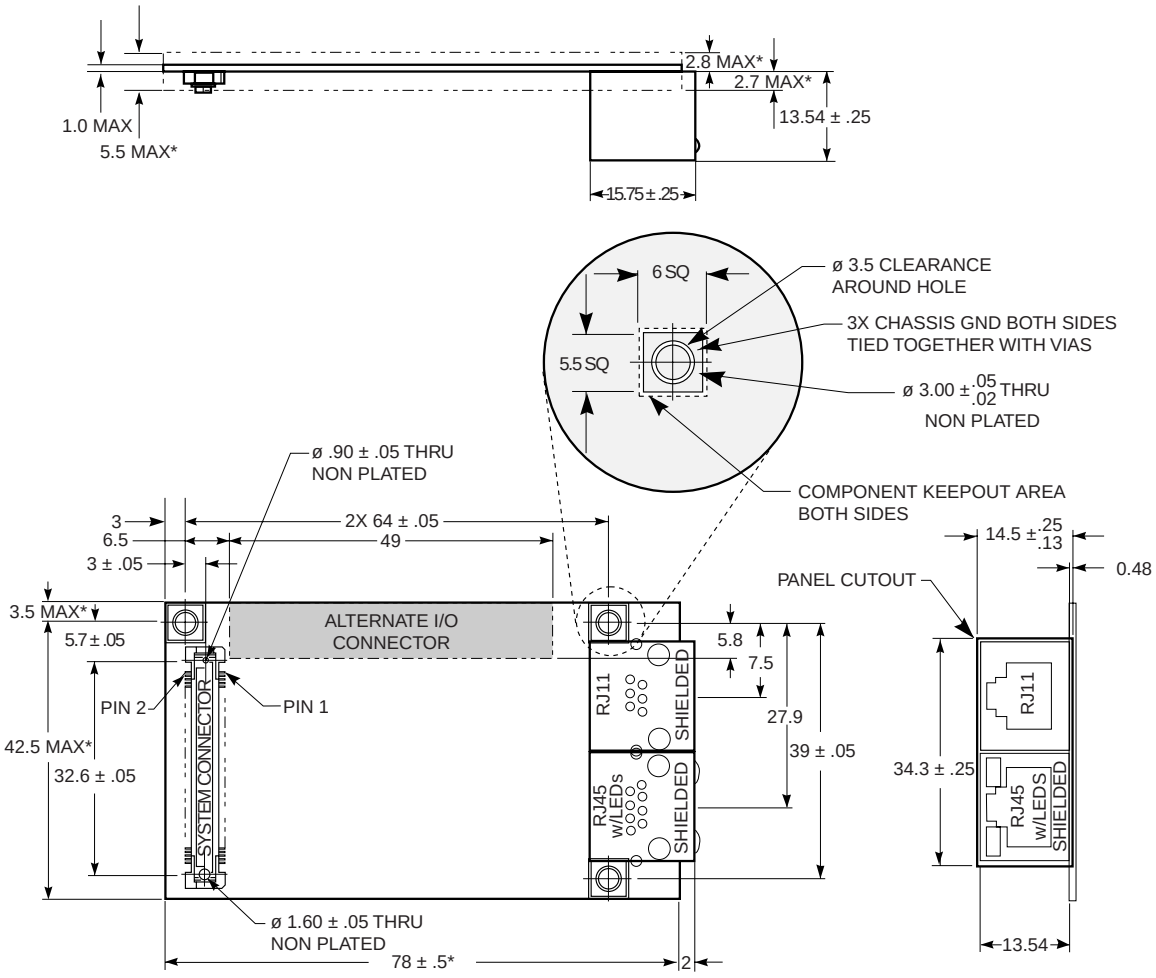


Figure 5-6: Type IIB Form Factor

5.4.5 Type IIIA Form Factor

The Type IIIA form factor supports a card that is not placed at the outer edge of the host system. The form factor for Type IIIA differs from that of Type IIIB in that Type IIIA has a larger Y dimension. The form factor for Type IIIA is further characterized by the following guidelines:

- All dimensions are in millimeters, unless otherwise specified.
- All dimension tolerances are ±.15 mm, unless otherwise specified.
- Dimensions marked with an asterisk (*) are overall envelope dimensions and include space allowances for insulation to comply with regulatory and safety requirements.
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads.
- Although Figure 5-7 illustrates a Type IIIA configuration with both a modem and a LAN connector, acceptable configurations are for modem only, LAN only, and LAN and modem combinations (as shown). The location of each connector remains the same for each configuration.

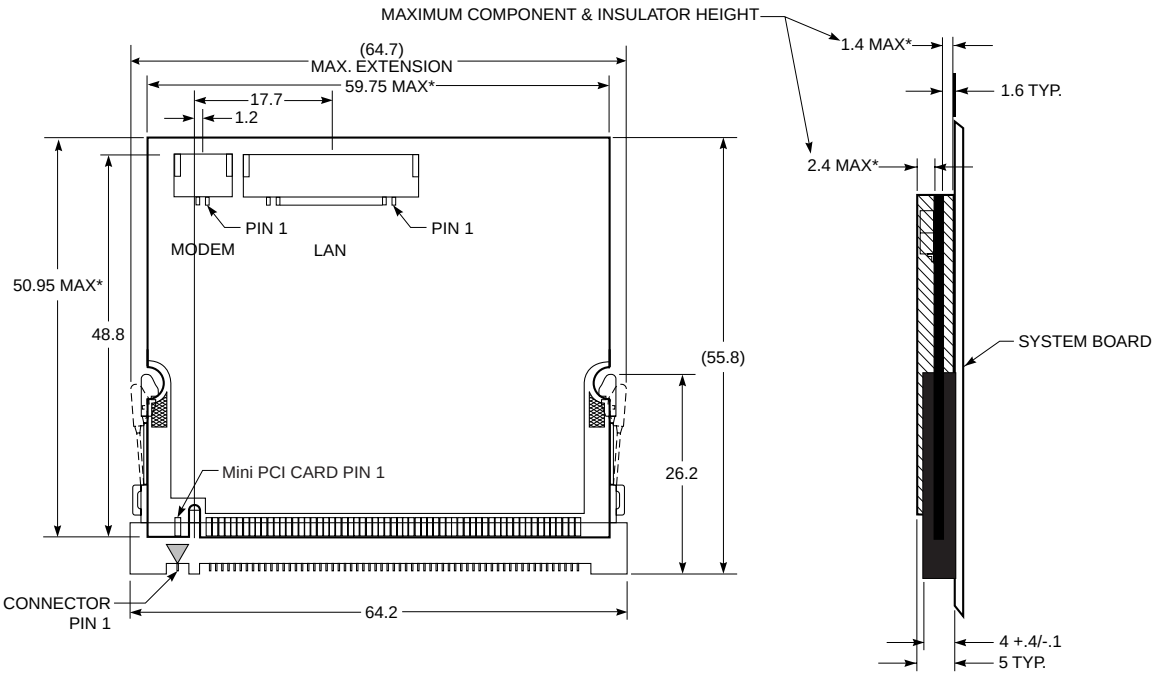


Figure 5-7: Type IIIA Form Factor

5.4.6 Type IIIB Form Factor

The Type IIIB form factor supports a card that is not placed at the outer edge of the host system. The form factor for Type IIIB differs from that of Type IIIA in that Type IIIB has a smaller Y dimension. The form factor for Type IIIB is further characterized by the following guidelines:

- All dimensions are in millimeters, unless otherwise specified.
- All dimension tolerances are ±.15 mm, unless otherwise specified.
- Dimensions marked with an asterisk (*) are overall envelope dimensions and include space allowances for insulation to comply with regulatory and safety requirements.
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads.
- Although Figure 5-8 illustrates a Type IIIB configuration with both a modem and a LAN connector, acceptable configurations are for modem only, LAN only, and LAN and modem combinations (as shown). The location of each connector remains the same for each configuration.

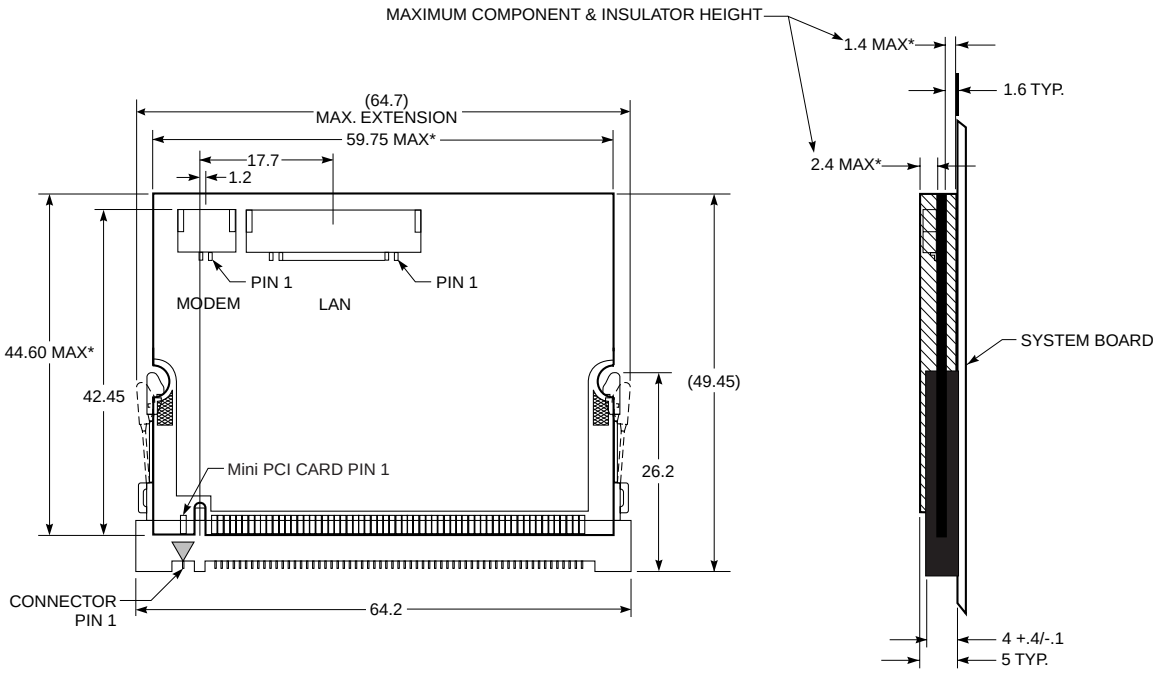


Figure 5-8: Type IIIB Form Factor

5.4.7 Type III PCB Details

Since the Type III form factor uses a card edge connector, the following drawings provide the printed circuit board (PCB) details required to fabricate a Type III Card. The Type III PCB is characterized by the following guidelines:

- All dimensions are in millimeters, unless otherwise specified.
- All dimension tolerances are ±.15 mm, unless otherwise specified.
- Edge contact pads (see Figure 5-15) on the top and bottom of PCB shall be electroless gold plating 0.05 μm Min. over electroless NI plating 2 μm Min. Figure 5-9 shows the Type III PCB form factor.
- Insulating material shall not interfere with or obstruct mounting holes or grounding pads.
- The EMC grounding pads shall have a conductive finish and be non-corrosive with the latch arms. See Figure 5-11 and Figure 5-14 for more information.

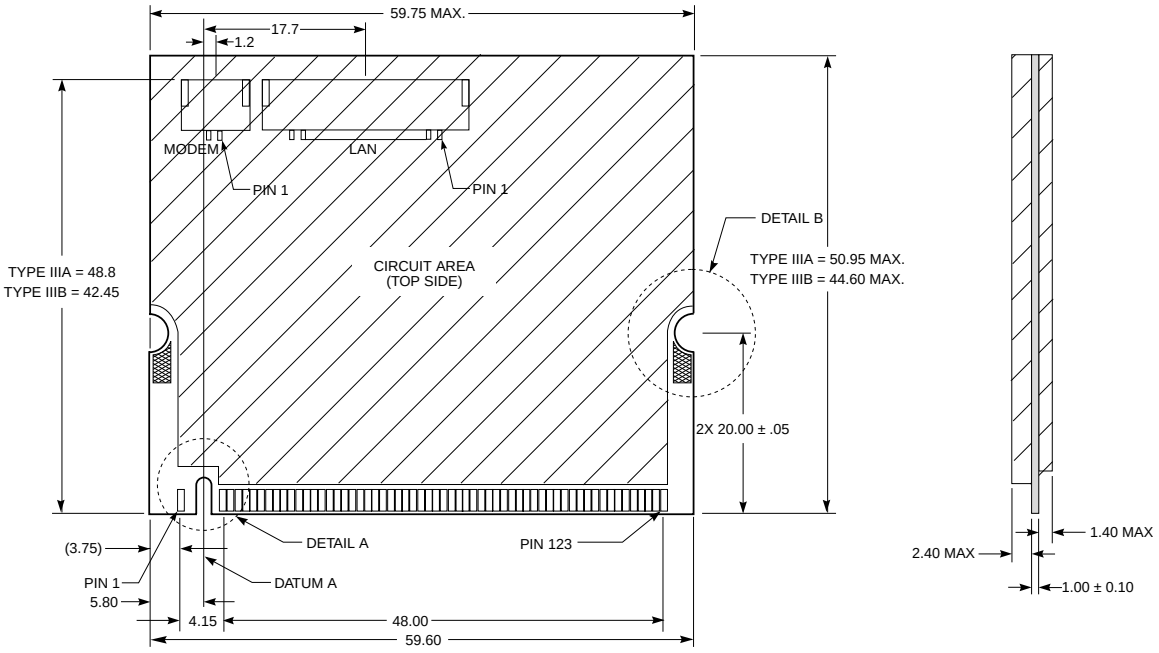


Figure 5-9: Type III PCB Form Factor

Figure 5-10 shows some detail from the top side of the Type III PCB.

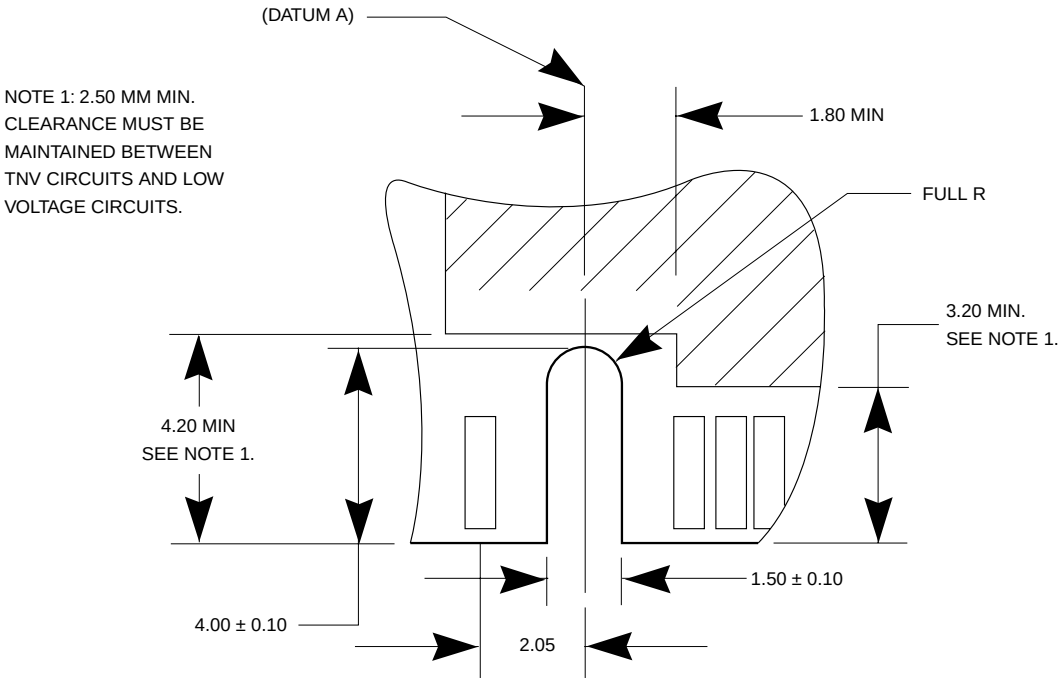


Figure 5-10: Type III PCB, Top Side, Detail A

Figure 5-11 shows some additional detail from the top side of the Type III PCB.

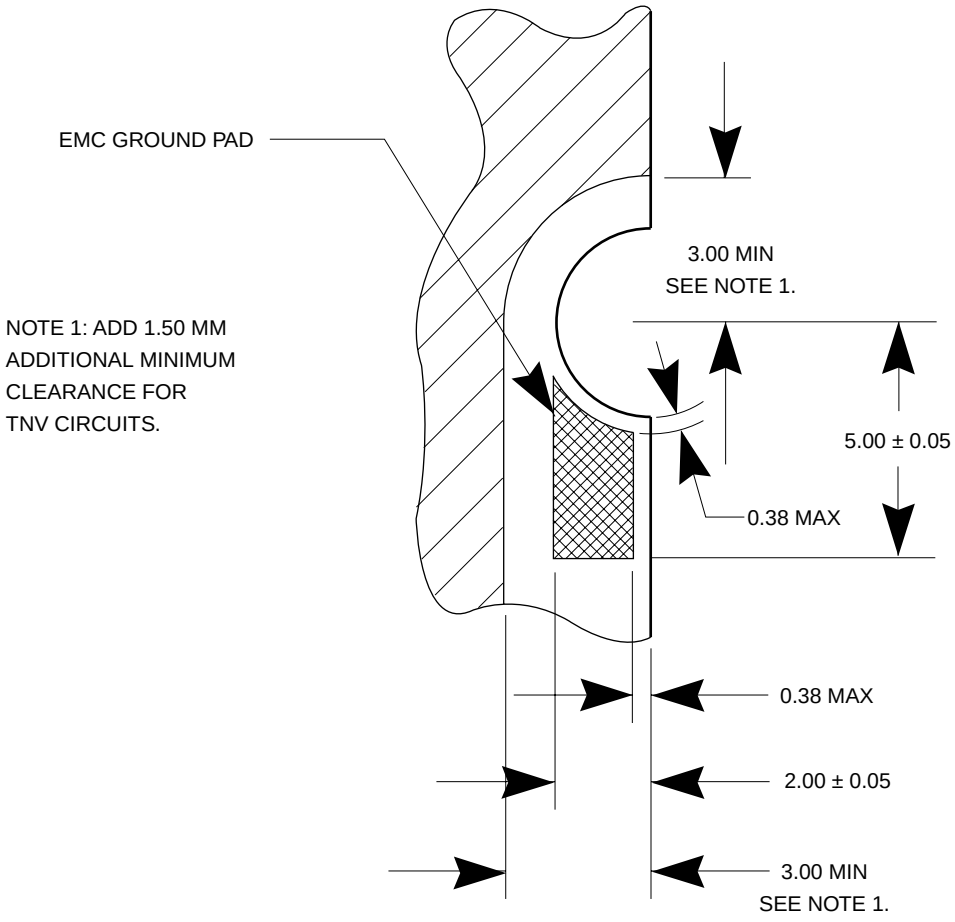


Figure 5-11: Type III PCB, Top Side, Detail B (2X)

Figure 5-12 shows the bottom side of the Type III PCB.

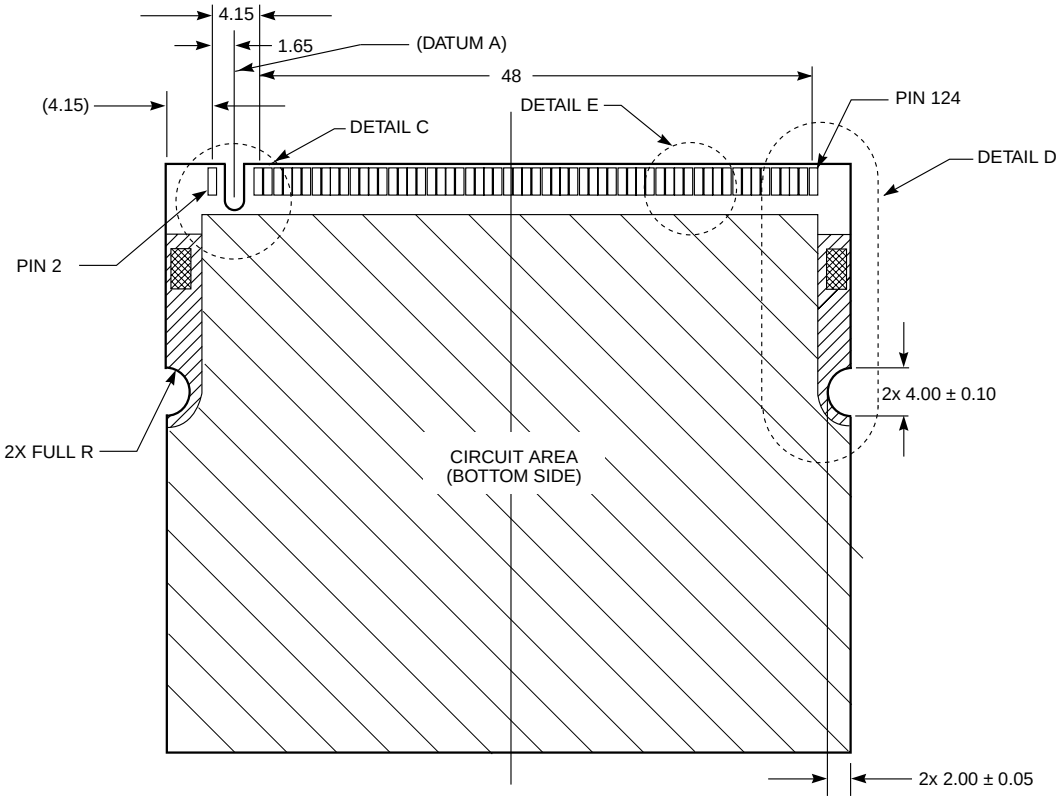


Figure 5-12: Type III PCB, Bottom Side

Figure 5-13 shows some details from the bottom side of the Type III PCB.

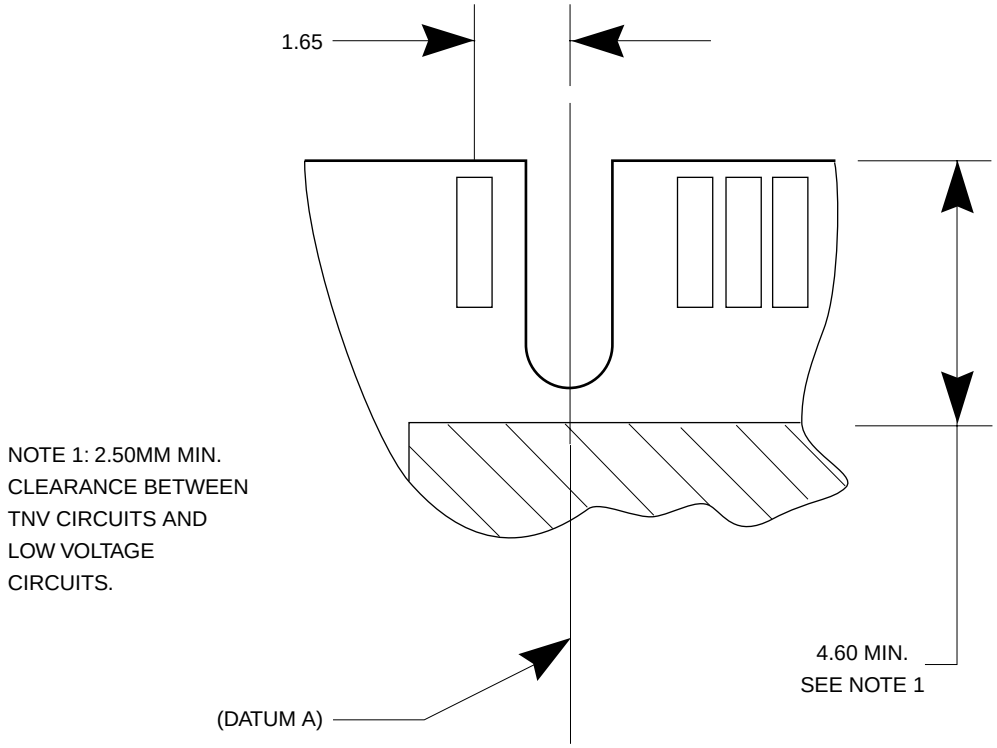


Figure 5-13: Type III PCB, Bottom Side, Detail C

Figure 5-14 shows final details of the bottom side of the Type III PCB.

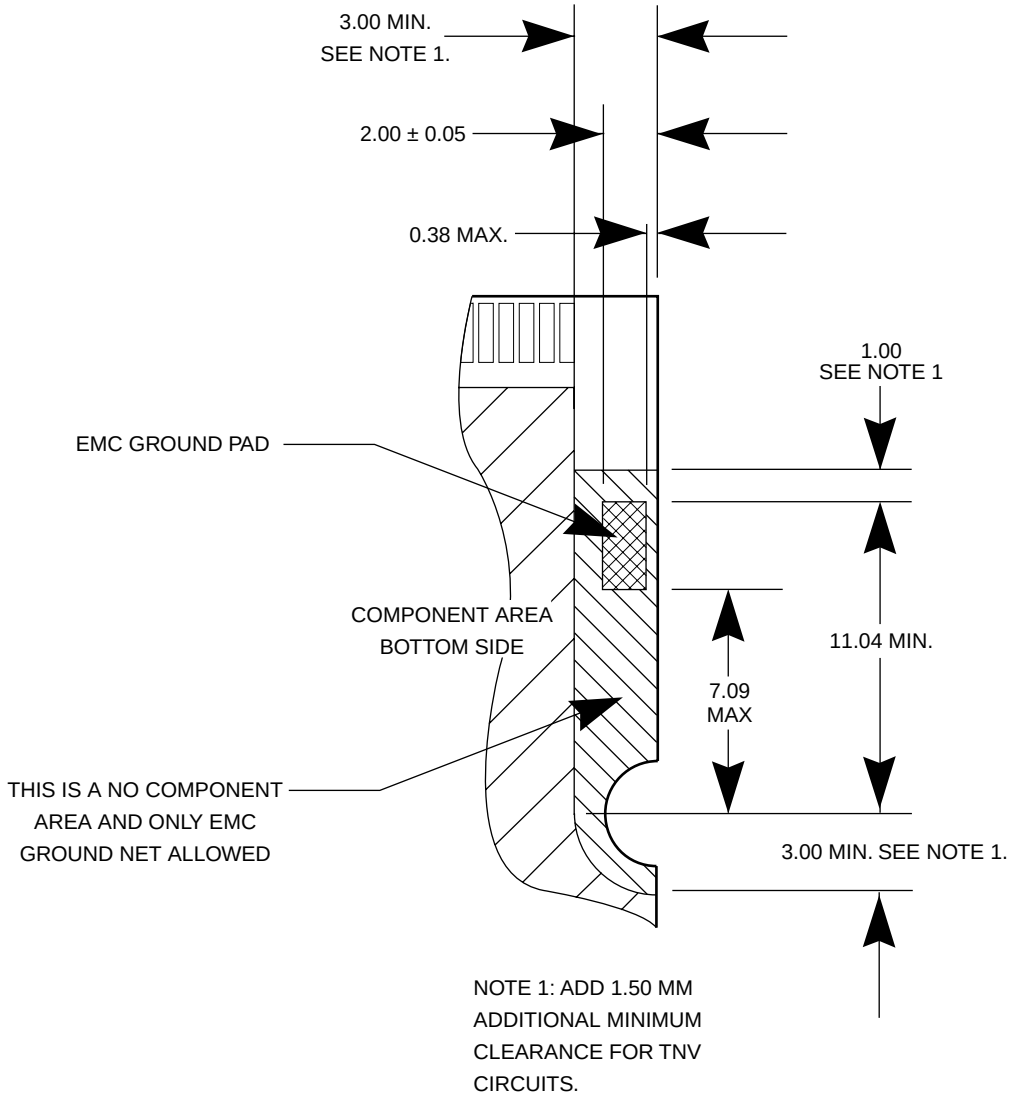


Figure 5-14: Type III PCB, Bottom Side, Detail D (2X)

Figure 5-15 shows contact finger detail for the Type III PCB.

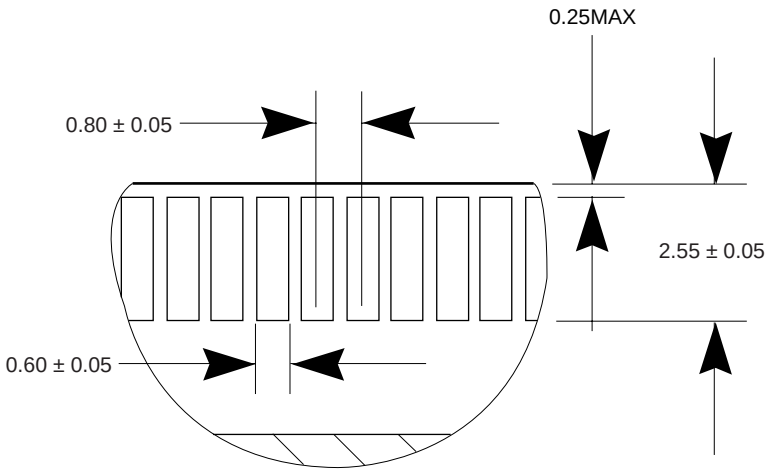


Figure 5-15: Type III PCB, Bottom Side, Detail E

5.5 Connector Information

This section describes the different types of connectors used by the three Mini PCI Cards. The connector types are system, I/O, and RJ.

5.5.1 System Connectors

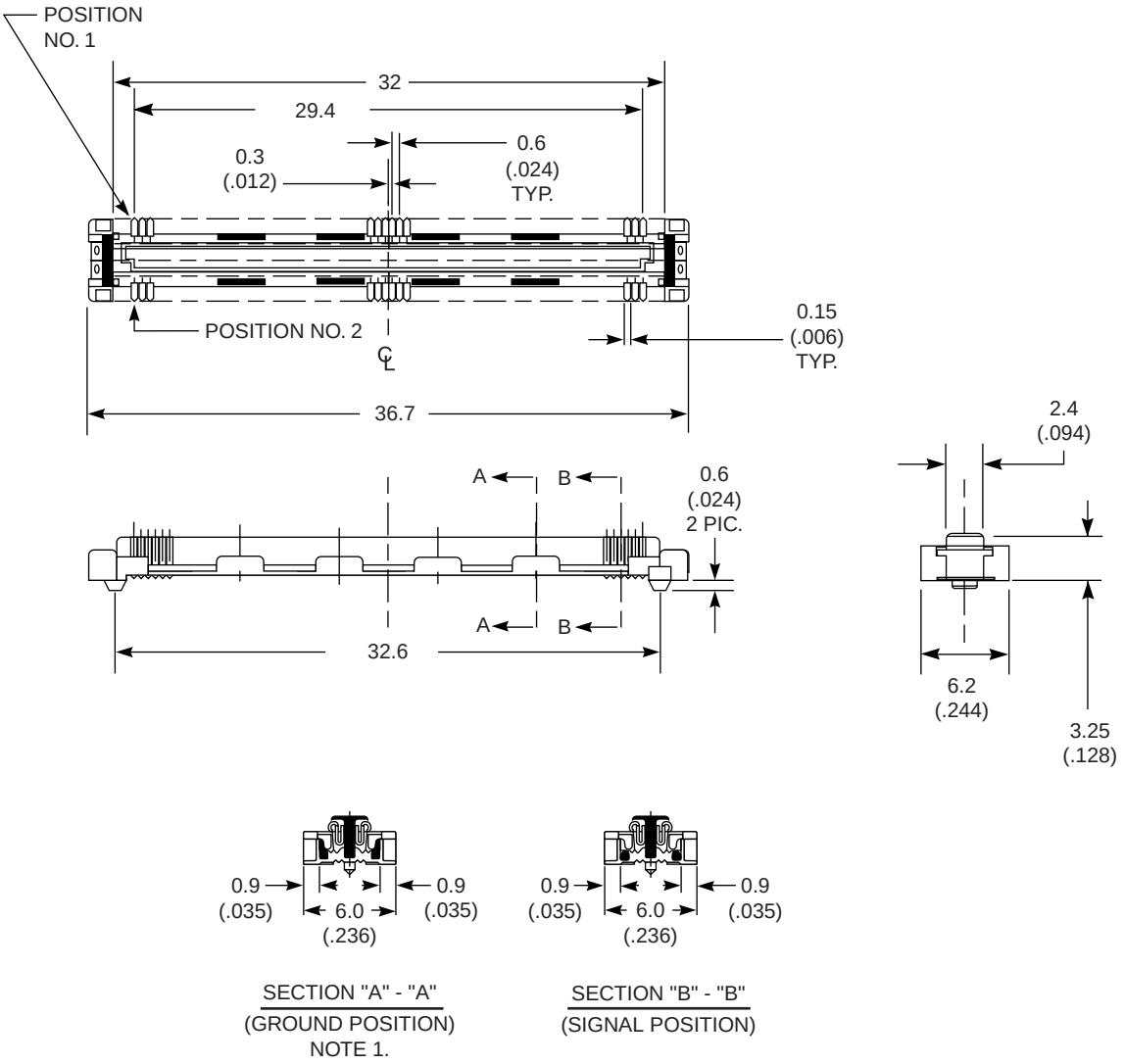
This section explains the system connector requirements for Types I, II, and III Mini PCI Cards.

5.5.1.1 Type I and Type II System Connector Specifications

The system connector for Type I and Type II consists of a 100 pin stacking type connector as shown in Figure 5-16.

The Amp 353183-8 100 position .6 mm Free Height plug or equivalent is located on the host system board. The Amp 353190-8 100 position .6 mm Free Height receptacle or equivalent is located on the Mini PCI Card. The overall stack height of the connector assembly is 4 mm as determined by the plug. Detailed dimensions should be obtained from the connector manufacturer.

Other connector stack heights are available from the connector manufacturers.



Note: 1) Ground contacts are used for signals and not as ground contacts.

Figure 5-16: Type I and Type II System Connector

Table 5-2 shows the 100 pin connector physical requirements.

Table 5-2: 100-Pin Connector Physical Requirements

Parameter	Specification
Connector Housing	High temperature plastic 94V-0
Contacts: Receptacle	Copper alloy
Contacts: Plug	Copper alloy
Contact Finish: Receptacle	Gold over nickel
Contact Finish: Plug	Gold over nickel

Table 5-3 lists the 100 pin connector mechanical performance specifications.

Table 5-3: 100-Pin Connector Mechanical Performance Specification

Parameter	Specification
Durability	50 cycles not exceeding 20 milliohms increase in contact resistance
Total mating force	90.0 N maximum

Table 5-4 lists the 100 pin connector electrical performance specifications.

Table 5-4: 100-Pin Connector Electrical Performance Specification

Parameter	Specification
Contact Resistance	55 milliohms maximum (initial) per contact
Insulation Resistance	500 MΩ maximum (initial), 100 MΩ minimum (final)
Dielectric Withstanding Voltage	0.2 kV AC for 1 minute between adjacent circuits
Capacitance	5 pF maximum @ 1 kHz per contact
Current Rating	0.5 A per contact
Voltage Rating	50 V AC per contact

Table 5-5 lists the100 pin connector environmental performance specifications.

Table 5-5: 100-Pin Connector Environmental Performance Specification

Parameter	Specification
Operating Temperature	-40 °C to 85 °C
Thermal Shock	Reference 3.5.13 of Amp Product Specification 108-5468
Mixed Flowing Gas Test	Reference 3.5.17 of Amp Product Specification 108-5468

5.5.1.2 Type III System Connector Specifications

The system connector for Type III consists of a 124-pin card edge type connector that is similar to the SO-DIMM type.

The Amp 1318228-1 124 position 0.8 mm socket or equivalent is located on the host system board. Detailed dimensions should be obtained from the connector manufacturer. Figure 5-17 shows the Type III system connector with a Type IIIA card inserted.

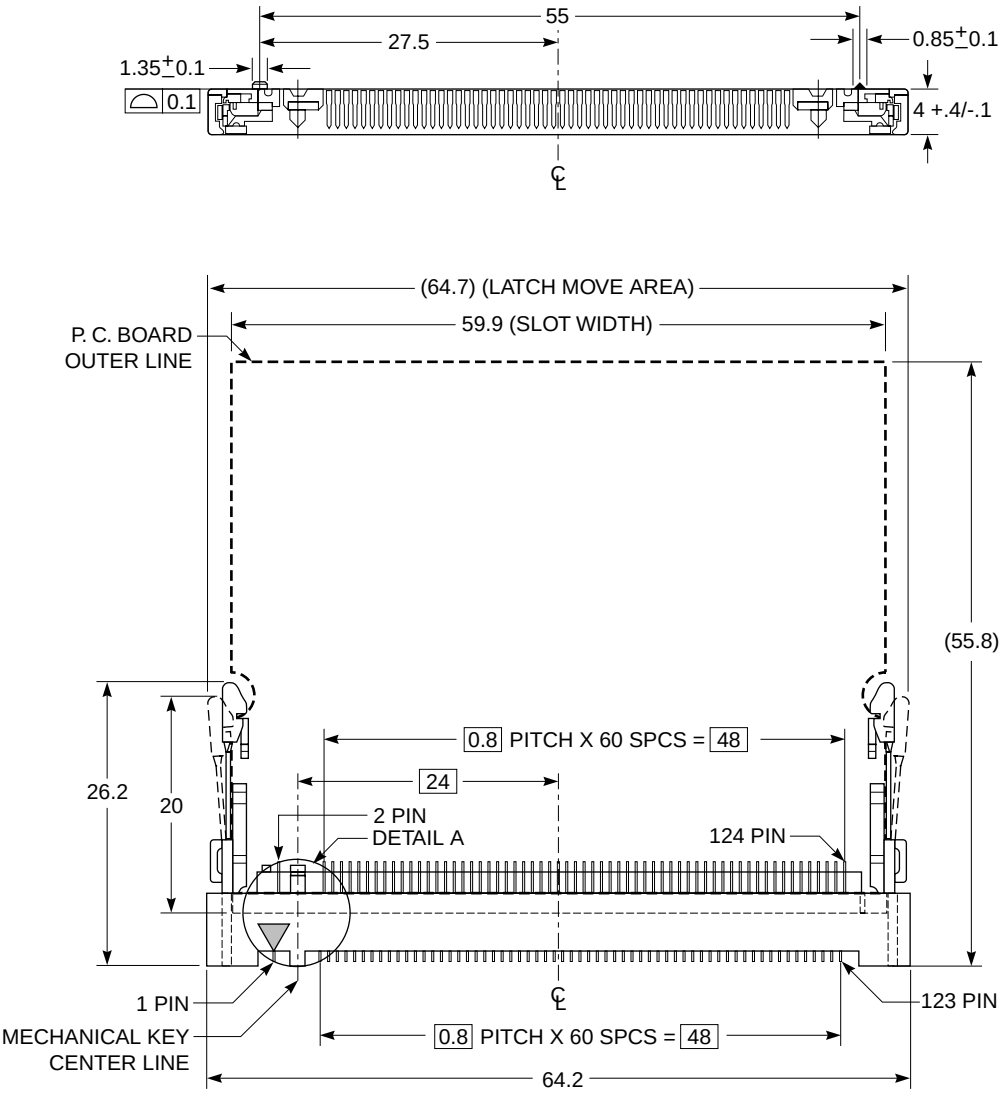


Figure 5-17: Type III System Connector (Shown with Type IIIA Card Inserted)

Table 5-6 shows the 124 pin connector physical requirements.

Table 5-6: 124-Pin Connector Physical Requirements

Parameter	Specification
Connector Housing	High temperature plastic 94V-0
Contacts: Receptacle	Copper alloy
Contact Finish: Receptacle	Gold over nickel

Table 5-7 lists the 124 pin connector mechanical performance specifications.

Table 5-7: 124-Pin Connector Mechanical Performance Specification

Parameter	Specification
Durability	50 cycles not exceeding 20 milliohms increase in contact resistance
Total mating force	51.5 N (5.3 Kgf) maximum

Table 5-8 lists the 124 pin connector electrical performance specifications.

Table 5-8: 124-Pin Connector Electrical Performance Specification

Parameter	Specification
Contact Resistance	55 milliohms maximum (initial) per contact
Insulation Resistance	500 MΩ maximum (initial), 100 MΩ minimum (final)
Dielectric Withstanding Voltage	0.2 kV AC for 1 minute between adjacent circuits
Capacitance	5 pF maximum @ 1 kHz per contact
Current Rating	0.5 A per contact
Voltage Rating	50 V AC per contact

Table 5-9 lists the 124 pin connector environmental performance specifications.

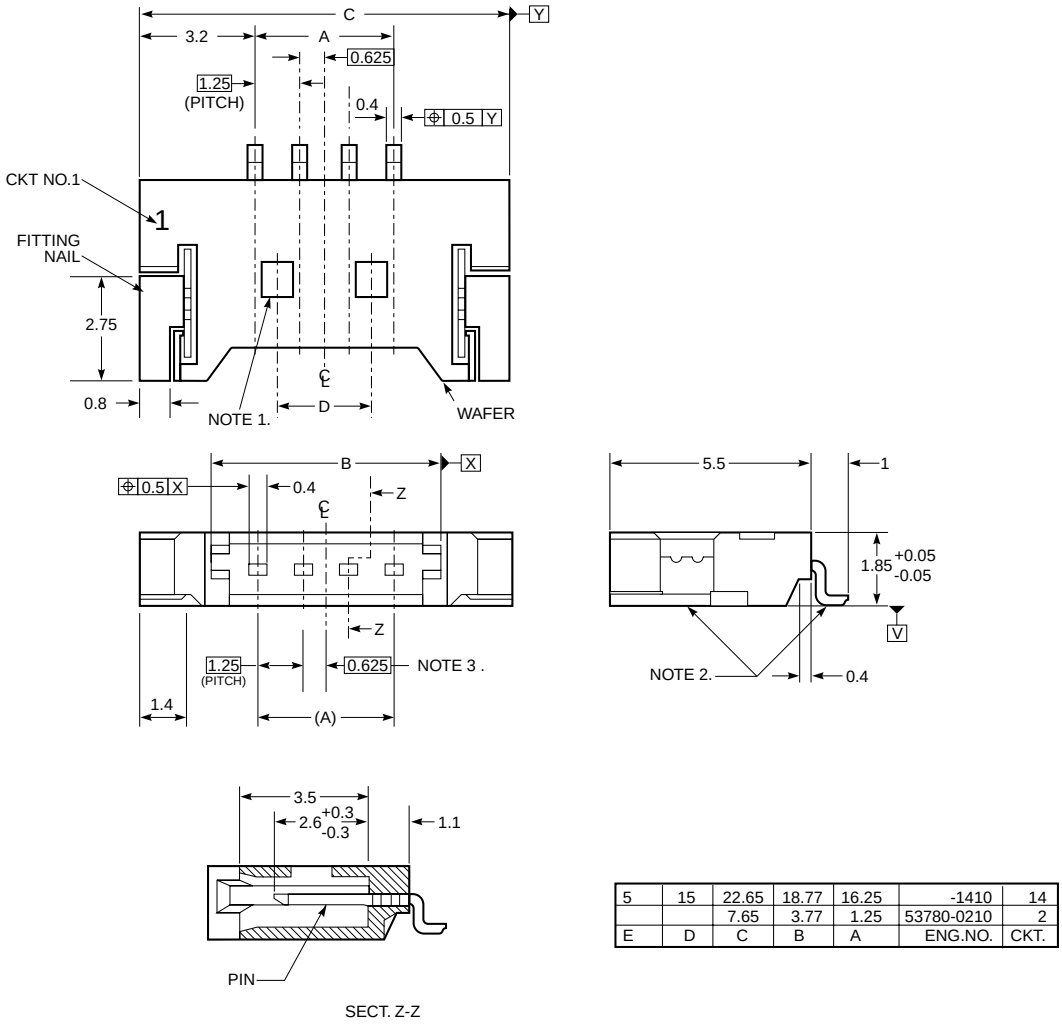
Table 5-9: 124-Pin Connector Environmental Performance Specification

Parameter	Specification
Operating Temperature	-40 °C to 85 °C
Thermal Shock	Reference 3.5.13 of Amp Product Specification 108-5468
Mixed Flowing Gas Test	Reference 3.5.17 of Amp Product Specification 108-5468

5.5.2 Type I and Type III LAN and Modem I/O Connectors

The LAN connector consists of a 14 pin wire/flex circuit to board type connector. The modem connector consists of a 2 pin wire/flex circuit to board type connector.

The Molex 53780 series or equivalent is located on the Mini PCI Card. The Molex 53780 series mates with either the Molex 51146 (wire) connector or the Molex 54281 (flex circuit) connector. Detailed dimensions should be obtained from the connector manufacturer. Figure 5-18 shows Type I and III I/O connectors.



5	15	22.65	18.77	16.25	-1410	14
		7.65	3.77	1.25	53780-0210	2
E	D	C	B	A	ENG.NO.	CKT.

Notes:

1. Locking window: one place for two and three circuit connectors and two places for more than three circuit connectors.
2. Misalignment of solder tail and fitting nail V from surface

   Upper direction 0.05 max.

   Lower direction 0.15 max.
3. Applies to even numbered circuit connectors.

Figure 5-18: Type I and Type III I/O Connectors

Table 5-10 shows the I/O connector physical requirements for Types I and II.

Table 5-10: I/O Connector Physical Requirements

Parameter	Specification
Connector Housing	PPHS 94V-0
Contacts	Phosphor Bronze
Contact Finish	Gold over nickel

Table 5-11 shows the I/O connector mechanical performance specifications for Types I and II.

Table 5-11: I/O Connector Mechanical Performance Specification

Parameter	Specification
Durability	30 cycles not exceeding 20 milliohms increase in contact resistance
Total mating force	2.1 N maximum per circuit

Table 5-12 shows the I/O connector electrical performance specifications for Types I and II.

Table 5-12: I/O Connector Electrical Performance Specification

Parameter	Specification
Contact Resistance	20 milliohms maximum (initial) per contact
Insulation Resistance	100 MΩ minimum
Dielectric Withstanding Voltage	0.25 kV AC for 1 minute between adjacent circuits
Current Rating	1.0 A per contact
Voltage Rating	125 V AC per contact

Table 5-13 shows the I/O connector environmental performance specifications for Types I and II.

Table 5-13: I/O Connector Environmental Performance Specification

Parameter	Specification
Operating Temperature	-40 °C to 85 °C

5.5.3 RJ Connectors for Type II Mini PCI Cards

The following list defines the characteristics of the RJ connectors for the Type II Mini PCI Card.

- Both connectors have the locking tabs in the up position.
- The RJ45 is available in shielded and unshielded configurations. The RJ11 is also available in shielded and unshielded configurations. Figure 5-19 illustrates both connectors in the shielded configuration. The outside dimensions of the RJ11 and the RJ45 are the same.
- The RJ45 supports LEDs.
- It is recommended that the RJ connectors be “through hole.” If surface mount RJ connectors are used, the retention force of the RJ connector to the Mini PCI Card should be comparable to the retention force of a "through hole" RJ connector to the Mini PCI Card. The surface mount electrical contacts shall be designed such that the contact solder joints shall maintain reliable contact through the normal mating and unmating with the RJ cable.
- The RJ11 and RJ45 interface dimensions shall comply with FCC Part 68, Subpart F.

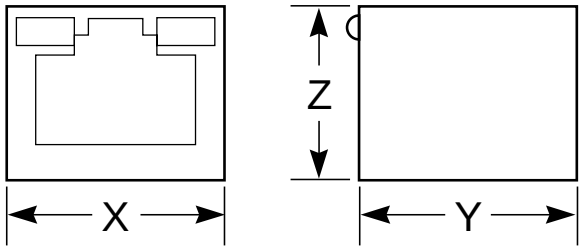


Figure 5-19: RJ Connector Detail

Table 5-14 shows representative connector part numbers from several suppliers.

Table 5-14: Representative Connector Information

Connector	Suppliers		
	AMP	Amphenol	Molex
RJ11	1339201-3	RJHS-7040-F1	44380-0003
RJ11 w/shield	1339202-3	RJHS-7K40-F1	44380-0006
RJ45 w/shield	1116509-4	RJHS-5K84-F1	44380-1010
X	16.26	16.51	16.38
Y	15.62	15.75	15.39
Z	13.35	13.46	13.54

The part numbers may differ depending on design requirements.

5.6 Thermal Guidelines

The Mini PCI Card manufacturer and system manufacturer must adhere to the following thermal guidelines in order to be compliant with this specification:

- The total system side power consumption of the Mini PCI Card must not exceed 2.0 W.
- The total system side power must be spread out relatively uniformly over the Mini PCI Card in order to avoid hot spots. The recommended maximum density of power dissipated is 0.057 W/cm^2 per side.
- The maximum ambient temperature of the air surrounding the non-powered Mini PCI Card (internal system temperature) shall not exceed 65 °C. The maximum rise in ambient temperature must not exceed 15 °C while running at maximum power.

Note: Additional heat beyond the 2.0 W of power consumption listed above may be generated by the Mini PCI Card's I/O circuitry due to modem line conditions in the approved countries. For example, TBR21 states a modem may dissipate as much as 2.4 W additional (40 V drop at 60 mA). If the Mini PCI Card requires additional thermal management in order to stay within the aforementioned criteria, the Mini PCI Card manufacturer must coordinate with the system manufacturer to achieve a final solution.

Chapter 6
Configuration Space

6.1 Configuration Space Organization

The Mini PCI Configuration Space implementation is that of a standard Type 00 header.

Since Mini PCI Cards are required to implement PCI bus power management, the Capabilities Support Bit, bit 4 in the PCI Status Register at offset 06h in the PCI Configuration Space, is set (1). The Capabilities Pointer at PCI Configuration Space offset 34h, which is used to point to the first Capabilities List data structure, is valid and nonzero.

PCI bus power management and the Power Management Capabilities Data Structure are defined in the *PCI Bus Power Management Interface Specification*.

It is strongly recommended that the Mini PCI Card power management implementation include the *PCI Bus Power Management Interface Specification*'s data registers for reporting device state DC power consumption and thermal dissipation.

Chapter 7
Power Management

7.1 Power Management for Mini PCI Cards

The Mini PCI Card implements power management as defined in the following specifications:

- *PCI Bus Power Management Interface Specification*
- *PCI Mobile Design Guide*
- *PC Card Standard–Electrical Specification*

Differences between the specifications and the Mini PCI Card power management specification are noted in Table 7-1.

Table 7-1: Mini PCI Power Management Exceptions

PCI Specification	Parameter	PCI Value	Mini PCI Value	Mini PCI Reference
PCI Bus Power Management Interface Specification	D0 uninitialized current	10 W	0.230 W	*PC Card Standard–Electrical Specification*
PCI Bus Power Management Interface Specification	Maximum 3.3VAUX current with PME enabled and PowerState bits set to state D3	375 mA	200 mA	*PC Card Standard–Electrical Specification*
PCI Bus Power Management Interface Specification	Maximum 3.3VAUX current in states D0, D1, and D2 for cards supporting $D3_{cold}$ wake events	375 mA	375 mA	*PCI Bus Power Management Interface Specification*

Table 7-1: Mini PCI Power Management Exceptions (continued)

PCI Specification	Parameter	PCI Value	Mini PCI Value	Mini PCI Reference
PCI Local Bus Specification	Maximum card power	25 W	2.0 W	*Mini PCI Specification*
PCI Bus Power Management Interface Specification	3.3VAUX current, PME not enabled, in state $D3_{cold}$	20 mA	5 mA	*Mini PCI Specification*

7.1.1 3.3VAUX Implementation

The decision to implement 3.3VAUX in a Mini PCI design is a non-trivial decision. The interrelationships that exist between several industry specifications must be understood and the commitment carries cost and complexity beyond just providing a 3.3V supply to the 3.3VAUX pin.

There are two power configurations supported by Mini PCI. The first is where 3.3VAUX is always provided to the connector, and the second is where 3.3VAUX is never supplied to the connector.

To the card vendor, this implies that a card may be built which hard connects its internal power rail to 3.3VAUX or 3.3V. The card vendor may also choose to integrate switches that allow sensing of the 3.3VAUX rail and, if present, switches permanently to the 3.3VAUX rail. This would allow a card to be placed in any Mini PCI compliant system.

To the system vendor, this implies a choice of $D3_{cold}$ support at the time that the system is designed. If $D3_{cold}$ is supported, then 3.3VAUX must always be provided. If $D3_{cold}$ support is not required, then 3.3VAUX may not be provided. The specifications involved include the bus specification (*PCI Local Bus Specification*) and its device power management specification (*PCI Bus Power Management Interface Specification*). There are also ramifications included in the *Advanced Configuration and Power Interface Specification* (ACPI) and, finally, requirements and recommendations within the *PC 99 System Design Guide* must be included.

This section will describe the interrelationships of these specifications and how they affect a Mini PCI design.

7.1.1.1 Industry Specification Definitions and Requirements

As defined in the *PCI Bus Power Management Interface Specification* and the *PCI Local Bus Specification*, the auxiliary supply voltage, 3.3VAUX, is optional. The requirement of 3.3VAUX came from the *PCI Bus Power Management Interface Specification's* support of a new concept called "wake events" from a new device state defined as $D3_{cold}$.

The device state $D3_{cold}$ is a further enhancement of the four device states defined in the *Advanced Configuration and Power Interface Specification.* Device states D0 through D3 all rely on the presence of system 3.3V. In the *PCI Bus Power Management Interface Specification*, the D3 state is refined into $D3_{hot}$ and $D3_{cold}$. $D3_{hot}$ is defined as the D3 state with 3.3V still applied and $D3_{cold}$ as the absence of 3.3V. It is the ability to provide wake events in which the host platform is not powered that defines device state $D3_{cold}$. $D3_{cold}$ is

defined as being the state in which the 3.3V supply is not present as described in Chapter 5 of the *PCI Bus Power Management Interface Specification.*

Because the ACPI specification only defines four states, support for $D3_{cold}$ events must be indicated in a different, dynamic method. All devices support ACPI's definition of $D3_{hot}$ by definition. Bus support for $D3_{cold}$ events requires special support from the PCI function and the host platform.

Support for PCI devices implementing $D3_{cold}$ support must be indicated to the operating system in a function independent PCI dependent method. Furthermore, it must be function specific; that is, it must be capable of indicating $D3_{cold}$ support for each independent function within a PCI multi-function implementation.

Within the constraints of the current ACPI and PCI Bus Power Management Interface specifications, it is clear that the only method available to indicate support for $D3_{cold}$ events for a specific PCI node is from that node's PCI Configuration Space.

PCI bus power management and, more specifically, implementation of 3.3VAUX is not required by the *PCI Bus Power Management Interface Specification*, the *PCI Local Bus Specification*, or the *PC 99 System Design Guide*. The *PC 99 System Design Guide* does state in Section 9.18 that if a platform supports S3 or S4 (which are options), it must provide support for 3.3VAUX. In Section 6.13 of the *PC 99 System Design Guide* mobile platforms are specifically excluded from being required to support remote wake-ups which would require the implementation of 3.3VAUX for PCI devices. In Section 2.2.7 of the *PCI Local Bus Specification*, the 3.3VAUX implementation is:

> "An optional 3.3 volt auxiliary power source delivers power to the PCI add-in card for generation of power management events when the main power to the card has been turned off by software.
>
> "The use of this pin is specified in the *PCI Bus Power Management Interface Specification*.
>
> "A system or add-in card that does not support PCI bus power management must treat the 3.3VAUX pin as reserved."

From the specifications reviewed, these conclusions can be drawn:

- Wake event support is optional.
- Wake event support for $D3_{cold}$ is optional even if general wake event support is implemented.
- If wake events are supported by the PCI Card, PCI bus power management implementation is required.
- If $D3_{cold}$ events are to be required from the PCI Card, 3.3VAUX support is required by the host platform.
- For the host platform, 3.3VAUX is optional if $D3_{cold}$ events are not supported.
- 3.3VAUX and 3.3V must be isolated power planes within the Mini PCI Card. The Mini PCI Card cannot connect 3.3VAUX to 3.3V.
- 3.3VAUX validity must be established during a PCI power up sequence in order to properly set bit 15 in Power Management Capabilities register.
- Removing 3.3VAUX is undefined.

In implementing the *PCI Bus Power Management Interface Specification*, Mini PCI allows for implementing and not implementing 3.3VAUX. Furthermore, in a mobile environment, there will be design choices made as to whether or not to support $D3_{cold}$

wake events depending on the main power source, either battery or AC. It is entirely reasonable to assume that value products which are very sensitive to cost pressures will choose not to implement $D3_{cold}$ wake event features. This parallels the *PC 99 System Design Guide* with respect to performance levels. Section 3.2.2 for Basic Requirements does not require S3 or S4 system states. Up the price point scale, products will feature $D3_{cold}$ support when on AC only but not support $D3_{cold}$ when on battery power. This is not a valid implementation in this specification. At the top of the pyramid, fully featured products will support $D3_{cold}$ wake events when on battery or AC. Mini PCI supports two of these three options. For each of the supported options, it is important to establish a reasonable set of conditions which govern the presence or absence or removal of the 3.3VAUX supply.

7.1.1.2 $D3_{cold}$ Support

In terms of $D3_{cold}$ support, there are three possible implementations, only two of these are valid. Each of these implementations, in turn, define valid price and performance goals of specific feature sets and requirements.

The first implementation to be discussed is the decision to not implement $D3_{cold}$ support under any conditions. This implementation represents the lowest level of complexity and least expensive option. For reasons of interoperability and in order to minimize market support, this option is not the preferred Mini PCI implementation for a system board.

Increased performance and cost introduces the implementation which will support $D3_{cold}$ only under certain conditions. In a mobile environment, this is frequently associated with power sources on AC or docked only, for example. This option is not supported by Mini PCI.

At the top of the performance/feature pyramid is the implementation which will support $D3_{cold}$ events under all conditions. Only when the battery is removed or exhausted and the system is not powered by AC would the system not supply 3.3VAUX. This is the preferred Mini PCI implementation model for host platforms.

The model that supports $D3_{cold}$ events in a mobile environment carries additional requirements not normally associated with the $D3_{cold}$ decision. This is because mobile environments will lose power and that event must be comprehended.

7.1.1.2.1 No $D3_{cold}$ Support

No $D3_{cold}$ support is defined for both the host platform and the PCI function. If the host platform does not support $D3_{cold}$ events, 3.3VAUX is not provided and the 3.3VAUX pin is a no connect per the *PCI Local Bus Specification*.

This is not the preferred Mini PCI implementation but it is a valid option. For the greatest interoperability success, the host platform must be designed to support $D3_{cold}$ wake-up events. Many Mini PCI Card implementations will be a port of desktop or similar solutions. In the desktop implementation, $D3_{cold}$ wake events are required for communications devices, and it is expected that this requirement will also soon be added to mobile platforms which is the targeted implementation for Mini PCI Cards.

It is not a requirement within the *PCI Local Bus Specification* or *PCxx System Design Guide* that cards designed to support $D3_{cold}$ wake events also function in platforms that do not support $D3_{cold}$ wake events. Furthermore, it is not a requirement that Mini PCI Cards that support $D3_{cold}$ wake events function in a platform that does not support $D3_{cold}$ wake events.

For platforms that do not support $D3_{cold}$ wake events from the Mini PCI function and choose not to implement 3.3VAUX, the 3.3VAUX pin must be left as a no connect. The platform vendor must work closely with the Mini PCI Card vendor to ensure that the Mini PCI design will not fail because of a lack of 3.3VAUX support.

7.1.1.2.2 System Board Supports $D3_{cold}$ Wake Events

In mobile products paralleling desktop functionality and feature sets, 3.3VAUX will be present at any time during normal operation. This is the preferred Mini PCI implementation for host platforms as it offers the greatest flexibility for end users and successful interoperability.

In these products, Mini PCI Cards supporting $D3_{cold}$ wake events would determine that 3.3VAUX is present and power the Mini PCI Card circuitry as appropriate to support $D3_{cold}$ wake events from the 3.3VAUX supply instead of the 3.3V supply. The Mini PCI Card would indicate in bit 15 of the PMC register found in the Mini PCI Card's PCI Configuration Space that $D3_{cold}$ wake events are supported with a "1".

The AC, 3.3VAUX, and 3.3V characteristics of system board designs supporting $D3_{cold}$ events under all conditions require that the transition from AC to no AC be seamless in terms of 3.3VAUX. That is, the 3.3VAUX must not fail to be present when the system transitions from AC to no AC as indicated in the Figure 7-1.

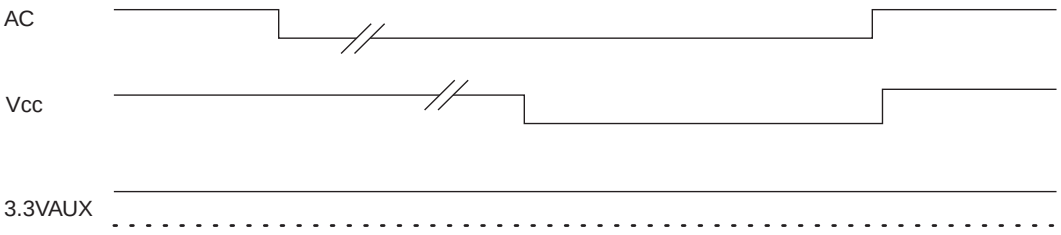


Figure 7-1: 3.3VAUX Always Supported

7.1.1.3 Guidelines For Handling Non-Standard 3.3VAUX Transitions

While not supported in this specification, in the sub-set of system implementations that support $D3_{cold}$ wake events but only when on AC power, the 3.3VAUX supply must be supplied and removed within a constrained environment that is hospitable to the Mini PCI Card and an ACPI compliant operating system.

The constrained environment is defined by the operating system's ACPI characteristics and the PCI bus power management. ACPI compliant operating systems determine support for $D3_{cold}$ wake events when devices are enumerated. It is not prudent to expect present operating system technology to determine $D3_{cold}$ support immediately prior to requesting this functionality. Therefore, 3.3VAUX transitions are limited to PCI power cycles and events which cause ACPI enumeration.

Two levels of functionality are possible in instances where $D3_{cold}$ support is implemented when AC is the power source. The first possibility removes the PCI function when AC is removed. This level of functionality would also require that the system force an enumeration sequence from the ACPI aware operating system in order to determine that the PCI function is no longer available. This sequence is illustrated in Figure 7-2. Implied in this implementation is the requirement that the PCI bus be isolated from the

PCI function that has been removed from operation. Isolation can take the form of physically isolating the PCI Card from the bus or the bus segment is in bus state B3.

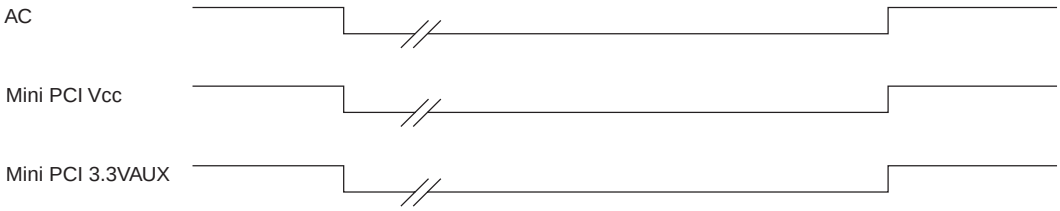


Figure 7-2: $D3_{cold}$ Support Only When On AC

The second possibility tries to return PCI functionality but without $D3_{cold}$ support. If it is required that the Mini PCI Card be returned to service, the Mini PCI Card must be sequenced through a new PCI power up sequence in order for the Mini PCI Card to properly initialize in the absence of 3.3VAUX as indicated in Figure 7-3. This will require that the Mini PCI Card also incorporate a detection mechanism to detect that 3.3VAUX is no longer available and an internal switch to switch its 3.3VAUX powered circuitry to be powered from 3.3V. This sequence would also require the host platform to cause an enumeration cycle to ensure that the operating system understand the change in the capabilities of the Mini PCI Card. Like the sequence above, when 3.3V is removed, the PCI bus must be isolated from the function. Clearly, when the PCI power sequence is initiated, a PCI reset sequence must accompany the power sequence.

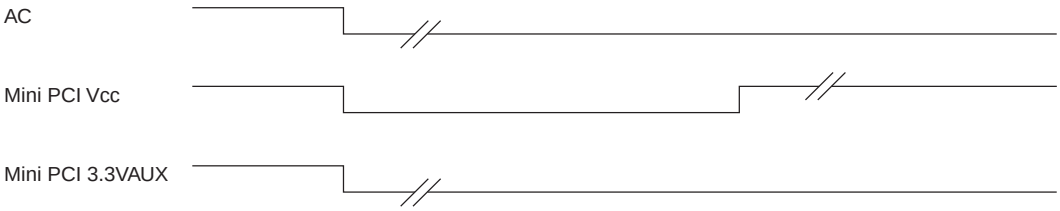


Figure 7-3: Re-establishment of Mini PCI Card Without 3.3VAUX Support

In either instance, if an extensive process is involved in making the decision as to whether or not to provide 3.3VAUX, the Mini PCI Card should be isolated from the PCI bus and the 3.3V and 3.3VAUX rails until the decision process is complete. The PCI power sequence must be implemented within the definition found in the *PCI Local Bus Specification* and the *PCI Bus Power Management Interface Specification*.

The option of supporting 3.3VAUX when on AC only and not supporting 3.3VAUX when on battery power is not a supported option in a Mini PCI implementation. The supported 3.3VAUX implementations are those in which 3.3VAUX is present all the time, preferred, or 3.3VAUX is never present.

As noted in the *PCI Bus Power Management Interface Specification*, the removal of 3.3VAUX is not addressed. A card's expected reaction to this sequence is undefined but, as currently defined, when 3.3VAUX and 3.3V are lost, it is reasonable to assume PME context is also lost. In a battery powered mobile environment, this instance will be a common occurrence.

Since the loss of 3.3VAUX is an undefined state, it will enhance most implementations if the loss of 3.3VAUX in system states S3, S4, or S5 can be determined in order to clean up those devices supporting $D3_{cold}$ events. Because PME context is "sticky" (refer to the *PCI Bus Power Management Interface Specification*), PME context must survive a PCI reset sequence. That is, the PCI bus segment reset sequence will not clear PME context.

Only a direct write to the PME_Enable and PME_Status bits will clear them. Also because they are "sticky," there is no guarantee that the bits will come up "0" or "1" with the application of 3.3V (and 3.3VAUX). If the loss of 3.3VAUX can be determined, the BIOS should clear PME context during the next PCI power sequence. This will ensure that the operating system does not find an errant wake event indication during operating system initialization.

There are two abnormal instances in which 3.3VAUX is lost or removed that must be examined. These instances are when 3.3V is present and when it is not present. When 3.3V is not present, PCI $D3_{cold}$ event support must be comprehended.

7.1.1.3.1 3.3VAUX Lost, 3.3V Present

The instance defined by 3.3VAUX being lost in the presence of 3.3V describes the worst case scenario for the Mini PCI Card as shown in Figure 7-4. If the card supports $D3_{cold}$ events, it most likely has some card functionality powered by 3.3VAUX and some functionality powered by 3.3V. It is required that 3.3VAUX not be removed when 3.3V is applied. Since it is possible to damage a Mini PCI Card implementing $D3_{cold}$ support, the loss of 3.3VAUX when 3.3V is valid must be addressed.

In this instance, losing 3.3VAUX must cause 3.3V to be removed and the Mini PCI Card must be isolated from the PCI bus.

If recovery is attempted, it must include a PCI power sequence with PCI bus segment reset and enumeration. Bus isolation must be implemented appropriately.

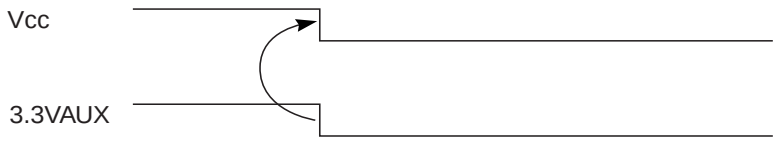


Figure 7-4: Loss of 3.3VAUX When 3.3V is Present

7.1.1.3.2 3.3VAUX Lost, 3.3V Not Present

If 3.3VAUX is lost and 3.3V is not present, two possibilities exist. These possibilities are that the PCI device was supporting $D3_{cold}$ events or it was not. In either case, it is not reasonable to assume that the host platform or the PCI function can recover from this instance without operating system support. In this instance, both 3.3V and 3.3VAUX should remain off until the user initiates a PCI power sequence.

7.1.1.3.3 3.3VAUX Transients

If the 3.3VAUX supply is removed when in an S4 or S5 state, it would be expected that a well designed host platform would not allow the reapplication of the 3.3VAUX supply prior to a normal PCI power cycle.

Referring to Figure 7-5, with the application of the system power switch, T_0, both 3.3V and 3.3VAUX are enabled to the Mini PCI Card. At time T_1, the Mini PCI Card enters a $D3_{cold}$ state. Some time later, for some system reason such as a low battery or the system is being serviced, the 3.3VAUX source supply is terminated. Another event, perhaps the system is docked or AC is applied, initiates the return of 3.3VAUX. The reapplication of 3.3VAUX in the absence of 3.3V constitutes an undefined sequence. This event is not unique to Mini PCI. It is precisely what occurs in a desktop environment when the AC is removed for purposes of inserting a card or some other service event. As an undefined state, it is not required, nor should it be expected, that a Mini PCI Card return to any previously defined state if 3.3VAUX is reapplied prior to a PCI power cycle. The Mini PCI Card must ensure that it does not enter a state that will damage the Mini PCI Card or the host system or assert the **PME#** signal. At time T_4, the system power switch is again initiated. A responsible system design would ensure that at time T_4, 3.3VAUX is removed and a valid PCI power cycle is executed (T_4 to T_5).

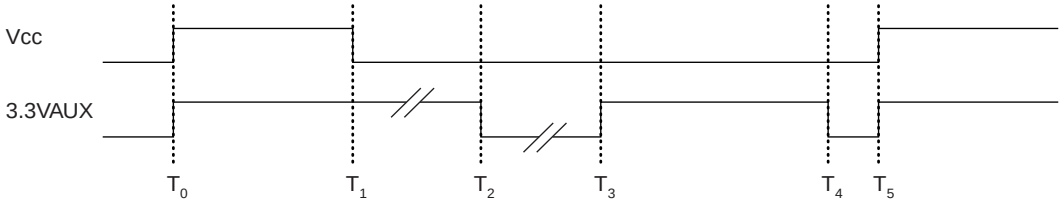


Figure 7-5: Undefined 3.3VAUX Transitions

7.2 Power Consumption

The maximum power allowed for any Mini PCI Card is 2.0 watts which represents the total power drawn from all power rails provided at the connector (5V, 3.3V, 3.3VAUX).

All host systems are expected to provide a full 2.0 watts to each Mini PCI system connector. Mini PCI Cards cannot consume more than 0.230 watts at power up or reset. An exception exists for the 0.230 watt power up limit. This exception allows a Mini PCI Card to consume 235 mA (0.775 watts) when a card is returning from the $D3_{cold}$ state with PME enabled. This allows for the combined requirements of supporting the PCI interface, configuration space, and the 200 mA allowed for functional requirements in supporting $D3_{cold}$ wake-up functionality. While in the reduced-power state, the board must provide full access to its PCI Configuration Space and must perform required function-specific bootstrap functions. All other board functions can be suspended if necessary. This power saving state can be achieved in a variety of ways, including the following two examples:

- Clock rates on the board can be reduced which reduces performance but does not limit functionality.
- Power planes to non-critical parts can be shut off with an electronic switch device which could limit functional capability.

The Mini PCI Card transitions from D0 uninitialized to D0 initialized power consumption level when the appropriate resource enable bits, in the PCI Configuration Space Command Register, are set. The Command Register controls a device's ability to generate and respond to PCI cycles. When a 0 is written to this register, the device is logically disconnected from the PCI bus for all accesses except configuration accesses. All devices are required to support this base level of functionality. Individual bits in the Command Register may or may not be implemented depending on a device's functionality. For instance, devices that do not implement an I/O Space probably will not

implement a writable element at bit location 0 of the Command Register. Devices typically power up with all zeroes in this register. The Command Register enable bits of interest are described in Table 7-2.

Table 7-2: Command Register Enable Bit

Bit Location	Description
IO Space Enable Bit 0 of the Command Register	Controls a device's response to I/O Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to I/O Space accesses. State after **RST#** is 0.
Memory Space Enable Bit 1 of the Command Register	Controls a device's response to Memory Space accesses. A value of 0 disables the device response. A value of 1 allows the device to respond to Memory Space accesses. State after **RST#** is 0.
Bus Master Enable Bit 2 of the Command Register	Controls a device's ability to act as a master on the PCI bus. A value of 0 disables the device from generating PCI accesses. A value of 1 allows the device to behave as a bus master. State after **RST#** is 0.

7.3 Optional PCI Implementations Required on Mini PCI Cards

Mini PCI Cards are required to implement the *PCI Mobile Design Guide's* clock run and the *PCI Bus Power Management Interface Specification's* 3.3VAUX.